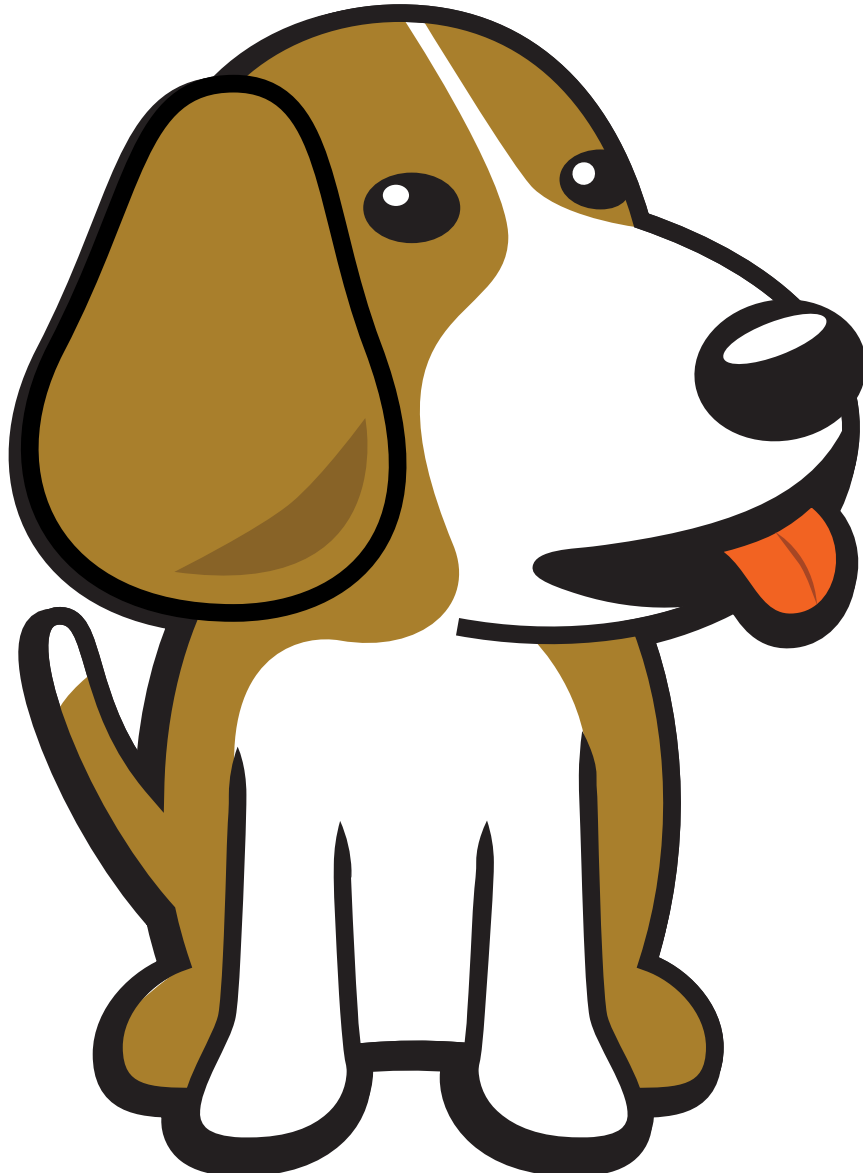




# BeagleV-Fire

Release 1.0.20240516-wip



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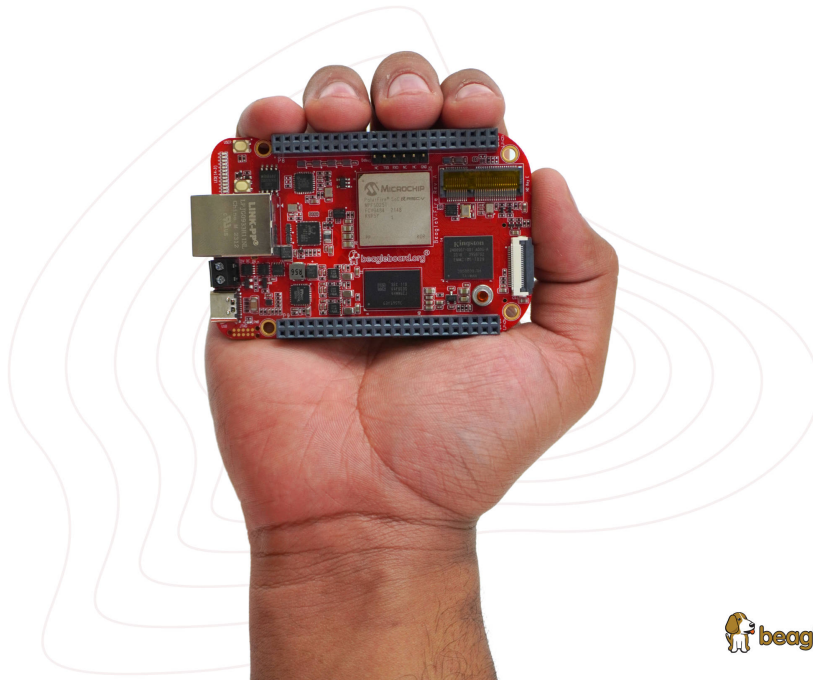
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BeagleV®-Fire is a revolutionary SBC powered by the Microchip's PolarFire® MPFS025T RISC-V System on Chip (SoC) with FPGA fabric. BeagleV®-Fire opens up new horizons for developers, tinkerers, and the open-source community to explore the vast potential of RISC-V architecture and FPGA technology. It has the same P8 & P9 cape header pins as BeagleBone Black allowing you to stack your favorite BeagleBone cape on top to expand it's capability. Built around the powerful and energy-efficient RISC-V instruction set architecture (ISA) along with its versatile FPGA fabric, BeagleV®-Fire SBC offers unparalleled opportunities for developers, hobbyists, and researchers to explore and experiment with RISC-V technology.

---

### License Terms

- This documentation is licensed under a [Creative Commons Attribution-ShareAlike 4.0 International License](#)
  - Design materials and license can be found in the [git repository](#)
  - Use of the boards or design materials constitutes an agreement to the boards-terms-and-conditions
  - Software images and purchase links available on the [board page](#)
  - For export, emissions and other compliance, see [Support](#)
  - All support for BeagleV Fire design is through BeagleBoard.org community at [BeagleBoard.org forum](#).
- 



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**Important:** This is a work in progress, for latest documentation please visit <https://docs.beagleboard.org/latest/>

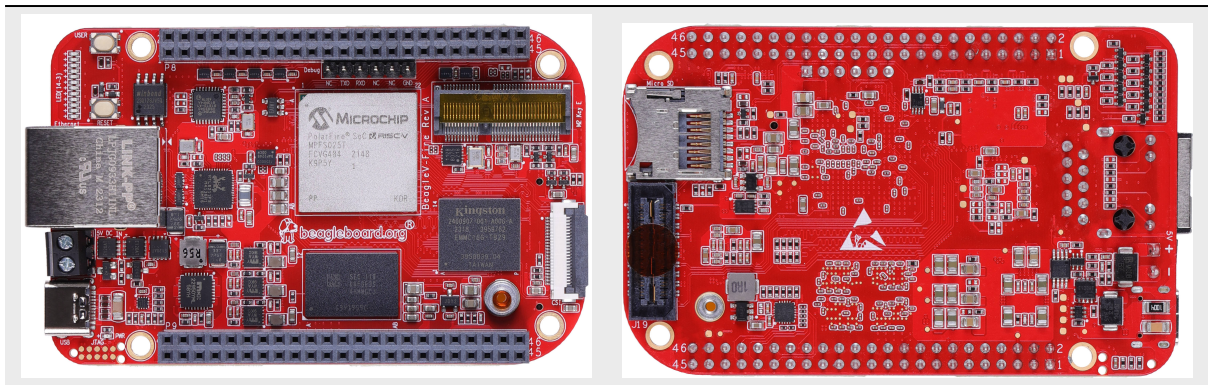
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# Chapter 1

## Introduction

BeagleV®-Fire is a revolutionary SBC powered by the Microchip's PolarFire® MPFS025T System on Chip (SoC) with 4x RV64GC Application cores, 1x RV64IMAC monitor/boot core, and FPGA fabric. BeagleV®-Fire opens up new horizons for developers, tinkerers, and the open-source community to explore the vast potential of RISC-V architecture and FPGA technology. It has the same P8 & P9 cape header pins as BeagleBone Black allowing you to stack your favourite BeagleBone cape on top to expand it's capability. Built around the powerful and energy-efficient RISC-V instruction set architecture (ISA) along with its versatile FPGA fabric, BeagleV®-Fire SBC offers unparalleled opportunities for developers, hobbyists, and researchers to explore and experiment with RISC-V technology.



### 1.1 Pinout Diagrams

Choose the cape header to see respective pinout diagram.

P8 cape header

P9 cape header

# BeagleV-Fire

P8 cape header pinout

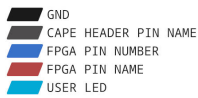
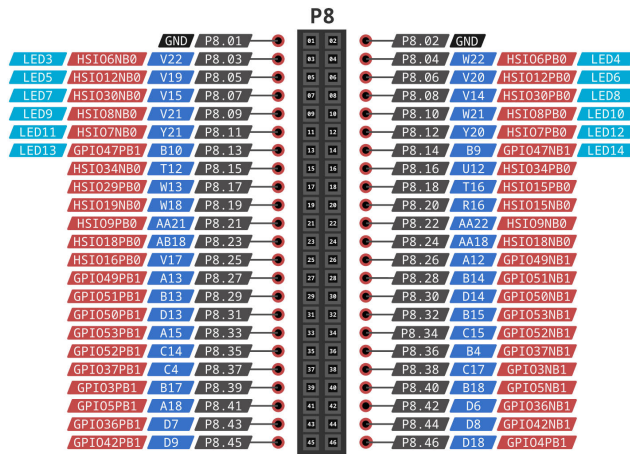
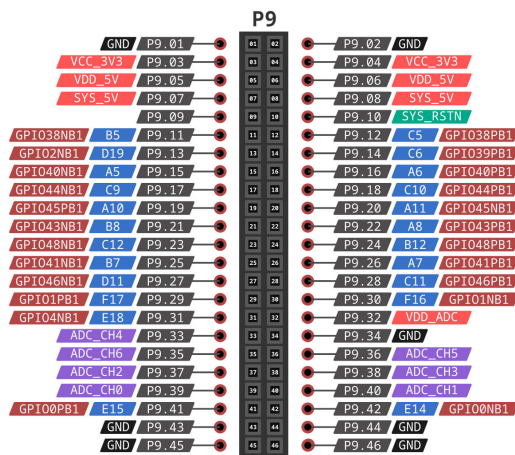


Fig. 1.1: BeagleV-Fire P8 cape header pinout

# BeagleV-Fire

P9 cape header pinout



- GND
- POWER
- CAPE HEADER PIN NAME
- FPGA PIN NUMBER
- FPGA PIN NAME
- ANALOG INPUT



Fig. 1.2: BeagleV-Fire P9 cape header pinout



## 1.2 Detailed overview

Table 1.1: BeagleV-Fire features

Feature	Description
Processor	MPFS025T-FCVG484E
Memory	2GB (1Gb x 16)- 1866MHz 3733Mbps, LPDDR4
Storage	Kingston 16GB eMMC
Wireless	1x M.2 Key E, support 2.4GHz/5GHz WiFi module
Ethernet	<ul style="list-style-type: none"> <li>PHY: Realtek RTL8211F-VD-CG Gigabit Ethernet phy</li> <li>Connector: integrated magnetics RJ-45</li> </ul>
USB C	<ul style="list-style-type: none"> <li>Connectivity: Flash/programming support</li> <li>Power: Input: 5V @ 3A</li> </ul>
Other connectors	<ul style="list-style-type: none"> <li>1x SYZYGY High speed connector</li> <li>microSD card slot</li> <li>CSI connector compatible with BeagleBone AI-64, BeagleV-Ahead, Raspberry Pi Zero / CM4 (22-pin)</li> </ul>

## 1.3 Board components location

This section describes the key components on the board, their location and function.

### 1.3.1 Front components location

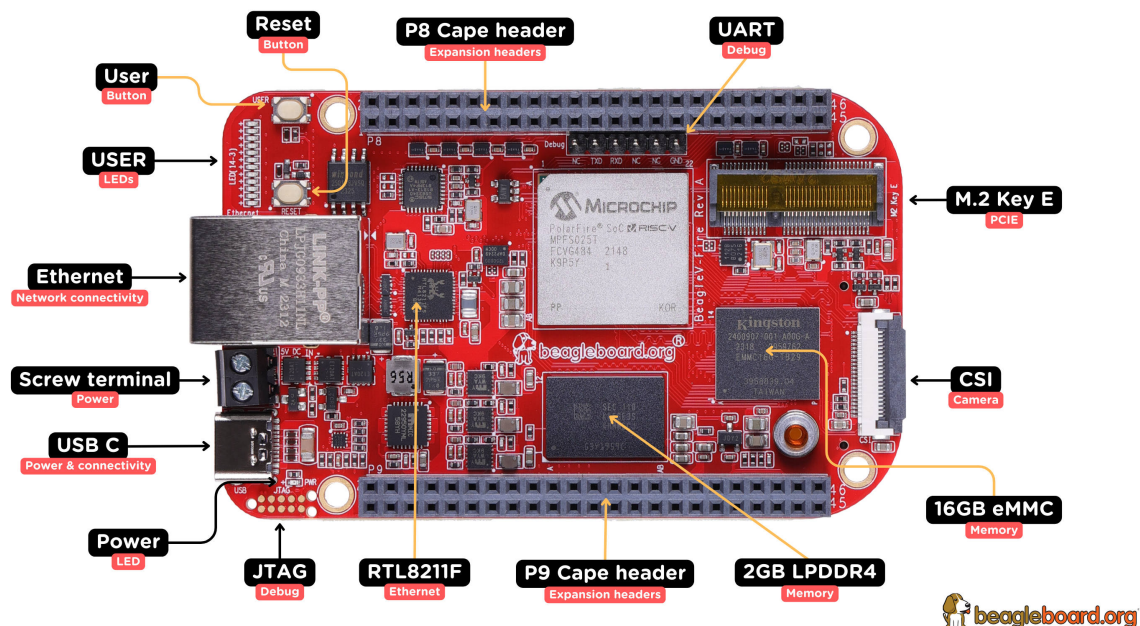


Fig. 1.3: BeagleV-Fire board front components location

Table 1.2: BeagleV-Fire board front components location

Feature	Description
Power LED	Power (Board ON) indicator
JTAG (MPFS025T)	MPFS025T SoC JTAG debug port
RTL8211F	Gigabit IEEE 802.11 Ethernet PHY
P8 & P9 cape header	Expansion headers for BeagleBone capes.
2GB RAM	2GB (1Gb x 16)- 1866MHz 3733Mbps, LPDDR4
16GB eMMC	Kingston 16GB eMMC Flash storage
CSI	22pin MIPI Camera connectors
M.2 Key E	PCIE M.2 Key E connector
UART debug header	6 pin UART debug header
Reset button	Press to reset BeagleV-Fire board (MPFS025T SoC)
User button	User defined (custom) action button
User LEDs	12x user programmable LEDs to show various board status during boot.
GigaBit Ethernet	1Gb/s Wired internet connectivity
Barrel jack	Power input
USB C	Power, connectivity, and board flashing.

### 1.3.2 Back components location

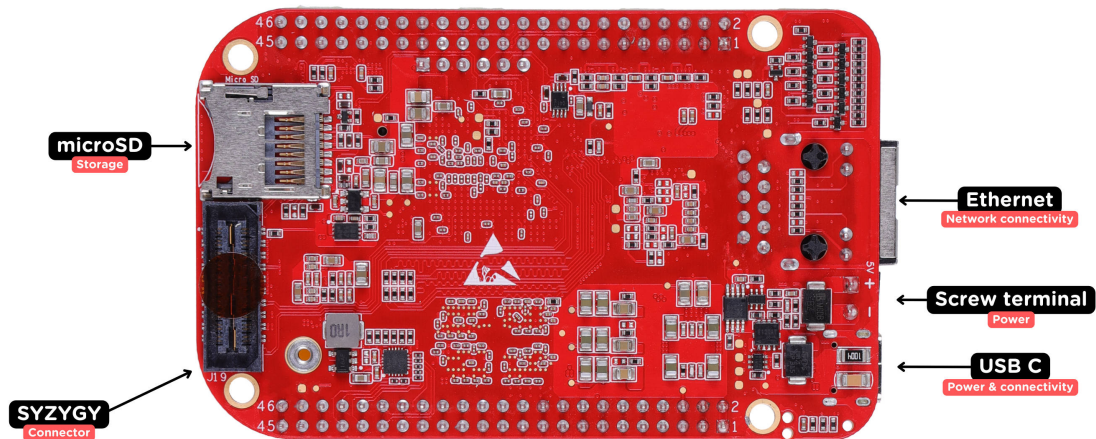


Fig. 1.4: BeagleV-Fire board back components location

Table 1.3: BeagleV-Fire board back components location

Feature	Description
microSD	microSD card slot
SYZYGY	SYZYGY High speed connector



## Chapter 2

# Quick Start

### 2.1 What's included in the box?

When you purchase a brand new BeagleV-Fire, In the box you'll get:

1. [BeagleV-Fire board](#)
2. Quick-start card

---

**Todo:** add image & information about box content.

---

---

**Tip:** For board files, 3D model, and more, you can checkout [BeagleV-Fire repository on OpenBeagle](#).

---

### 2.2 Unboxing

### 2.3 Tethering to PC

To connect BeagleV-Fire board to PC via USB Type C receptacle you need a USB type C cable. Connection guide for the same is shown below:

---

**Tip:** To get a USB type C cable you can checkout links below:

1. [USB C cable 0.3m \(mouser\)](#)
  2. [USB C cable 1.83m \(digikey\)](#)
- 

### 2.4 Flashing eMMC

#### 2.4.1 Flash the latest image on eMMC

### 2.5 Access UART debug console

---

**Note:** Some tested devices that are working good includes:

---



Fig. 2.1: <https://youtu.be/5cylv1R-1mc>



Fig. 2.2: BeagleV-Fire tethered connection

1. Adafruit CP2102N Friend - USB to Serial Converter
2. Raspberry Pi Debug Probe Kit for Pico and RP2040

To access a BeagleV-Fire serial debug console you can connect a USB to UART to your board as shown below:

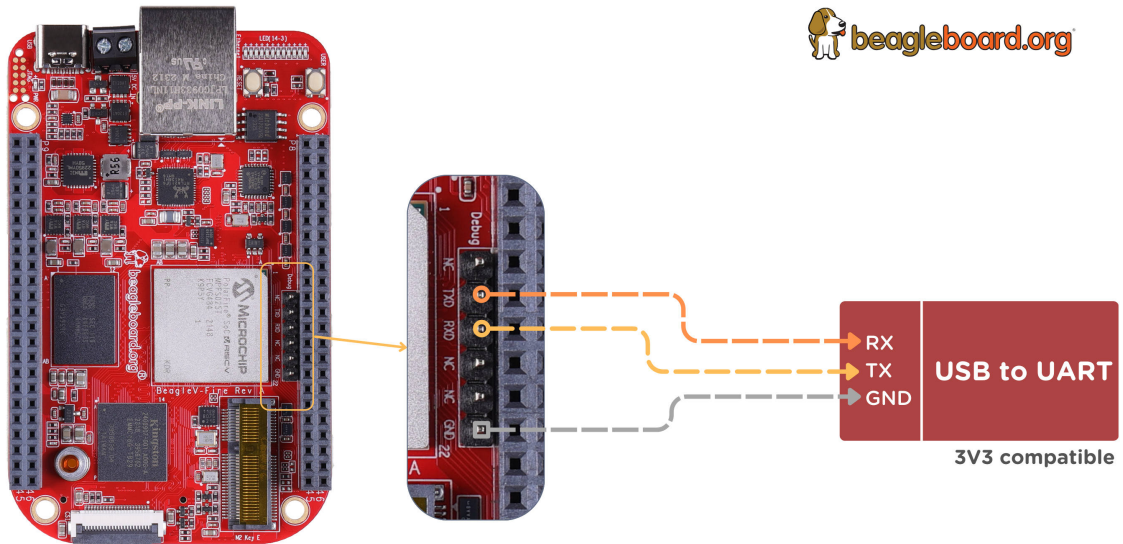


Fig. 2.3: BeagleV-Fire UART debug port connection

To see the board boot log and access your BeagleV-Fire's console you can use application like `tio` to access the console. If you are using Linux your USB to UART converter may appear as `/dev/ttyUSB0`. It will be different for Mac and Windows operating systems. To find serial port for your system you can checkout [this guide](#).

```
[lorforlinux@fedora ~] $ tio /dev/ttyUSB0
tio v2.5
Press ctrl-t q to quit
Connected
```

## 2.6 Demos and Tutorials

- [How to retrieve BeagleV-Fire's gateway version](#)
- [Upgrade BeagleV-Fire Gateway](#)
- [Flashing gateway and Linux image](#)
- [Gateway Design Introduction](#)
- [Microchip FPGA Tools Installation Guide](#)



# Chapter 3

## Design & specifications

If you want to know how BeagleV-Fire board is designed and what are its high-level specifications then this chapter is for you. We are going to discuss each hardware design element in detail and provide high-level device specifications in a short and crisp form as well.

**Tip:** For hardware design files and schematic diagram you can checkout BeagleV-Fire GitLab repository: <https://git.beagleboard.org/beaglev-fire/beaglev-fire>

### 3.1 Block diagram

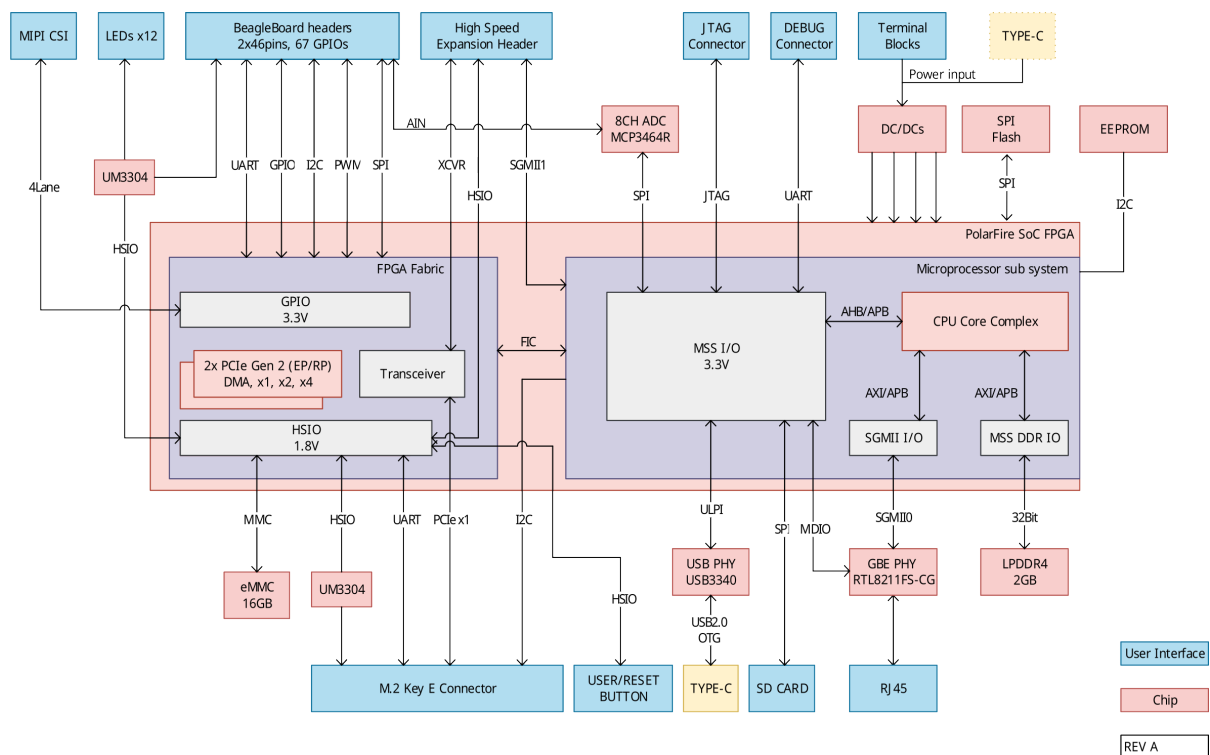


Fig. 3.1: System block diagram



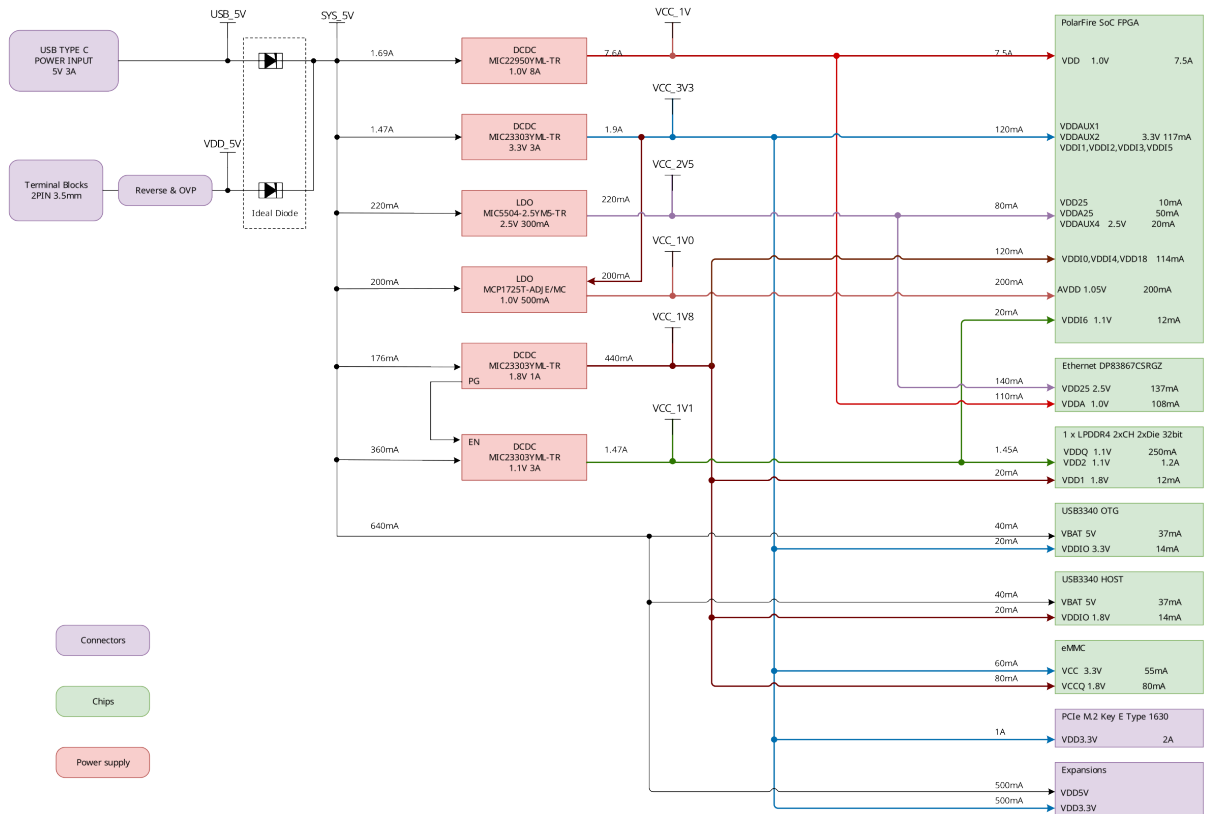


Fig. 3.2: Power tree diagram

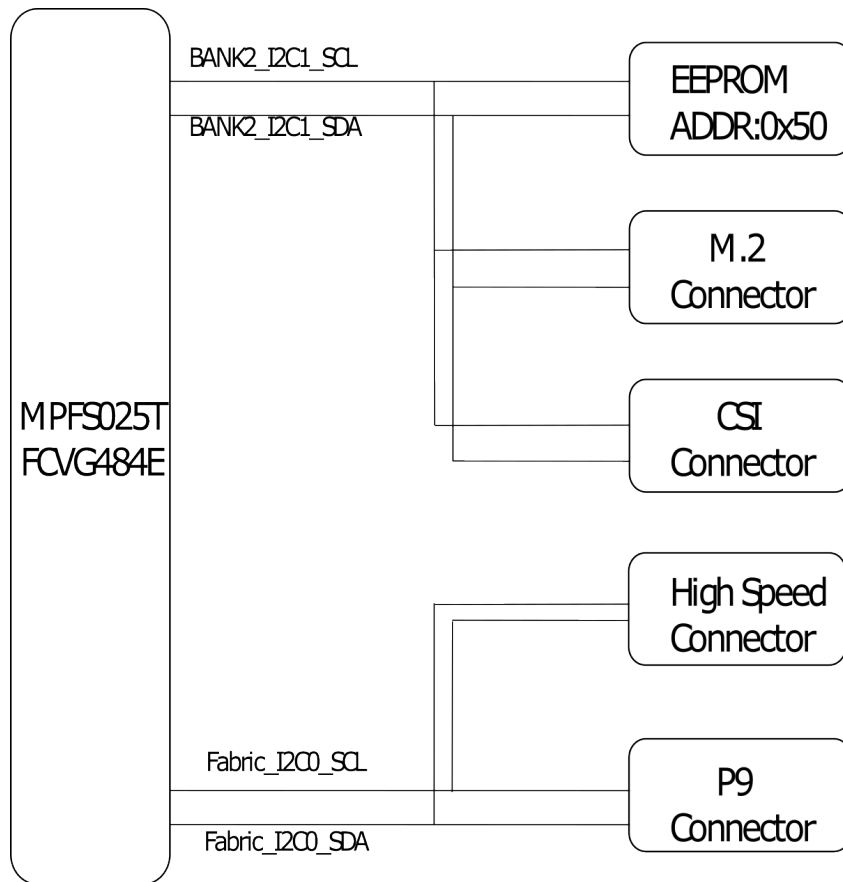


Fig. 3.3: I2C tree diagram

## 3.2 System on Chip (SoC)

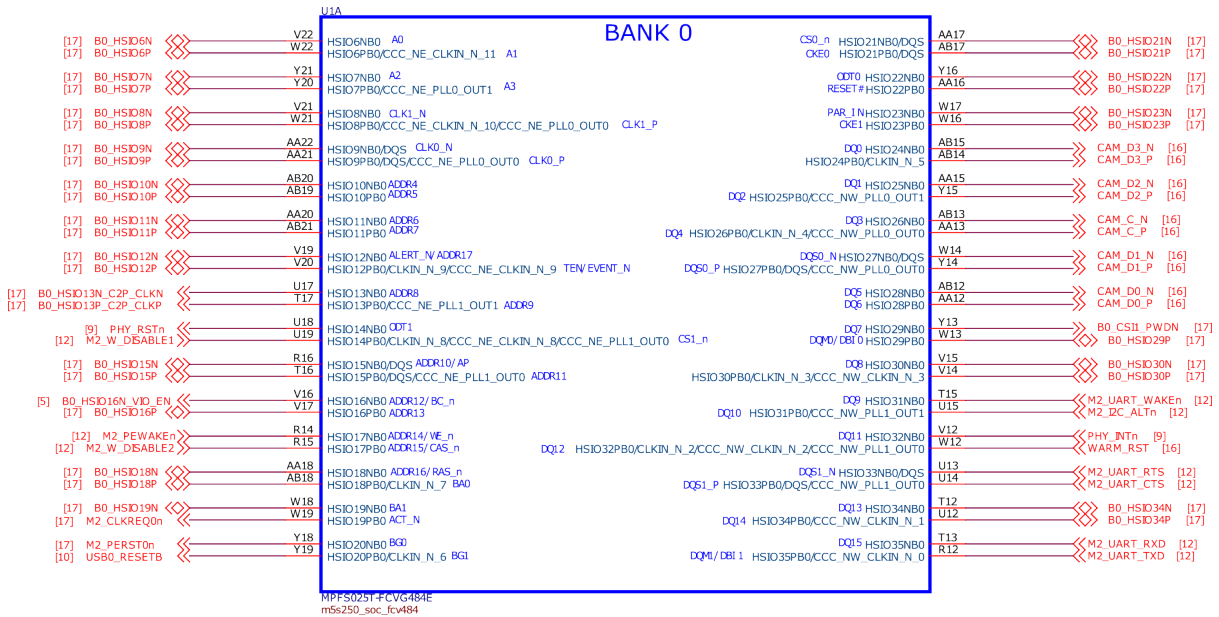


Fig. 3.4: SoC bank0

## 3.3 Power management

## 3.4 General Connectivity and Expansion

### 3.4.1 USB-C port

### 3.4.2 P8 & P9 cape header pins

### 3.4.3 ADC

## 3.5 Buttons and LEDs

### 3.5.1 User LEDs and Power LED

### 3.5.2 User and reset button

## 3.6 Connectivity

### 3.6.1 Ethernet

## 3.7 Memory, Media and Data storage

### 3.7.1 DDR memory

### 3.7.2 eMMC

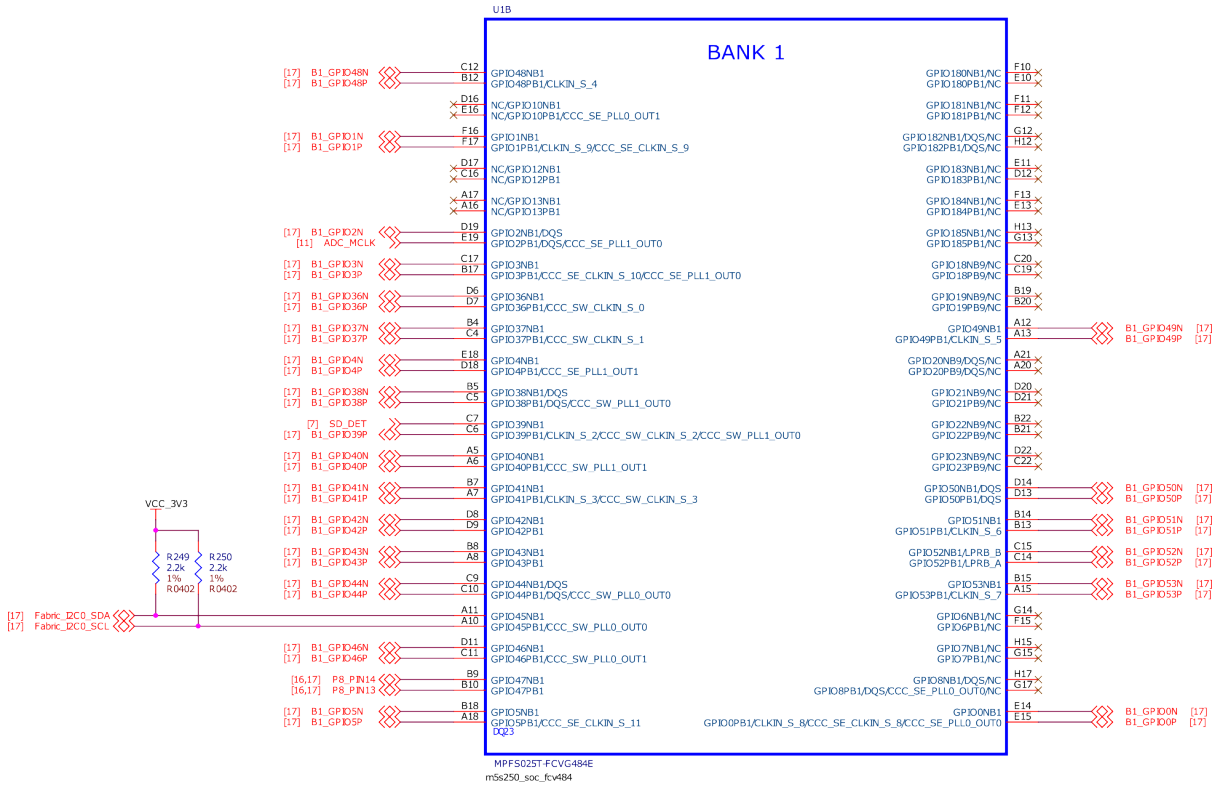


Fig. 3.5: SoC bank1

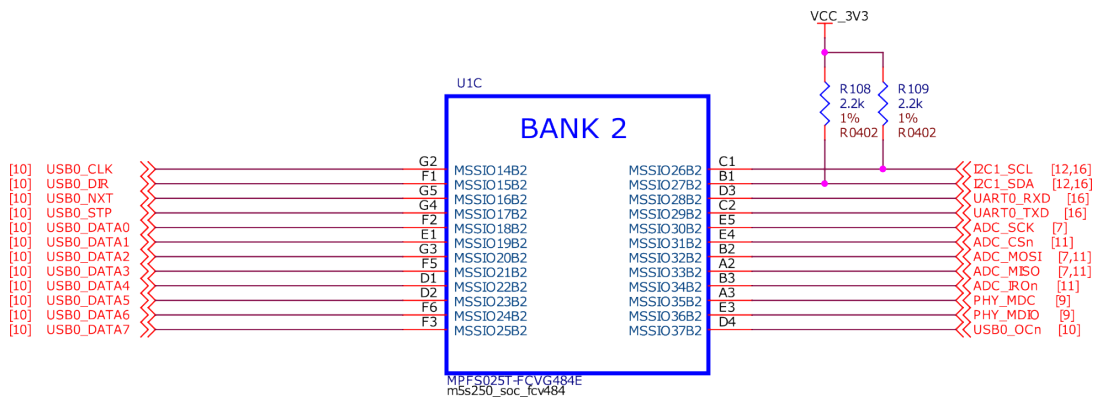


Fig. 3.6: SoC bank2

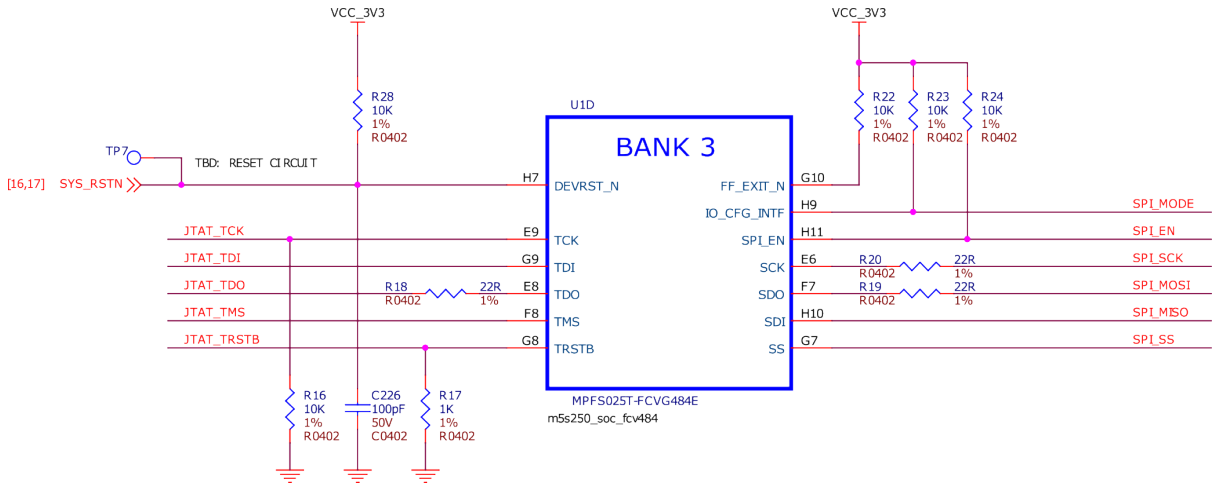


Fig. 3.7: SoC bank3

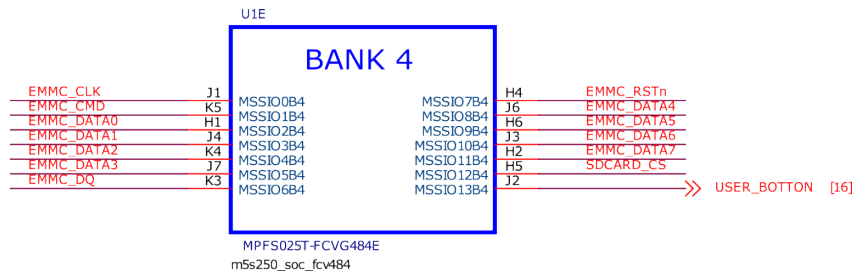


Fig. 3.8: SoC bank4

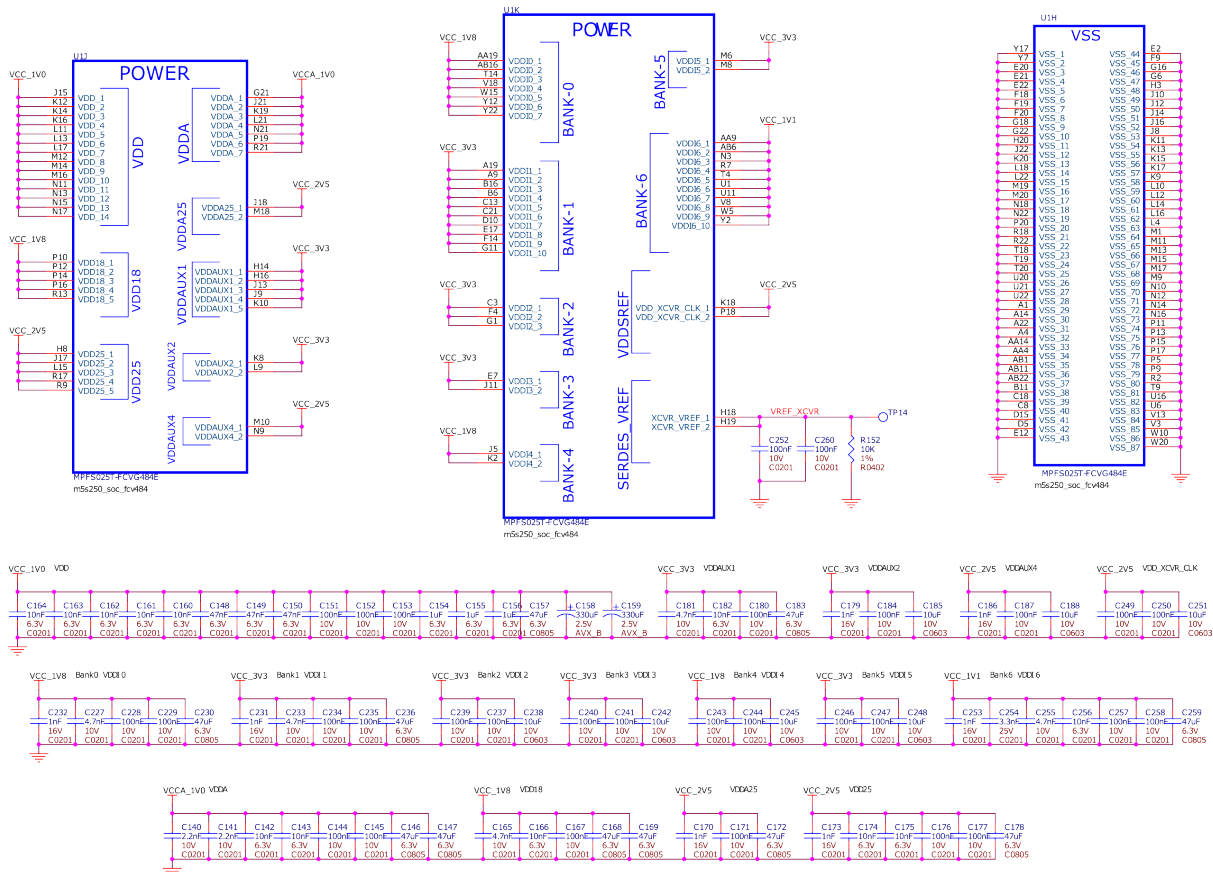


Fig. 3.9: SoC power

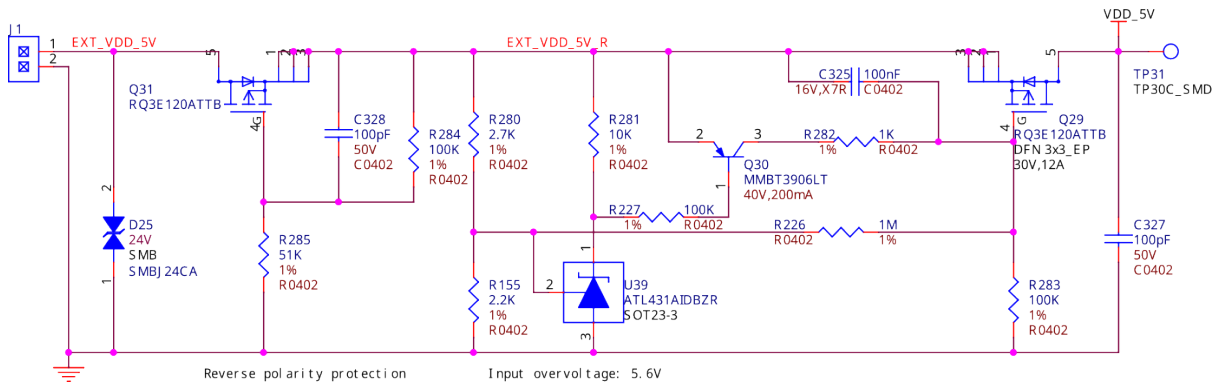


Fig. 3.10: DC 5V input

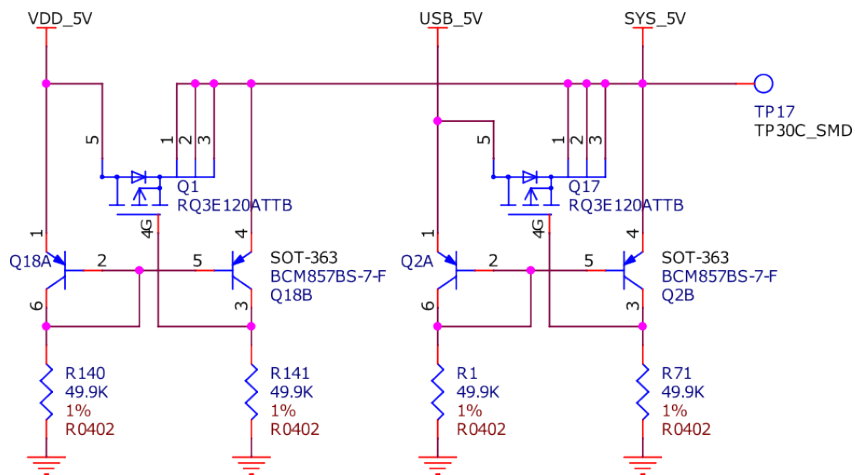


Fig. 3.11: Ideal diode

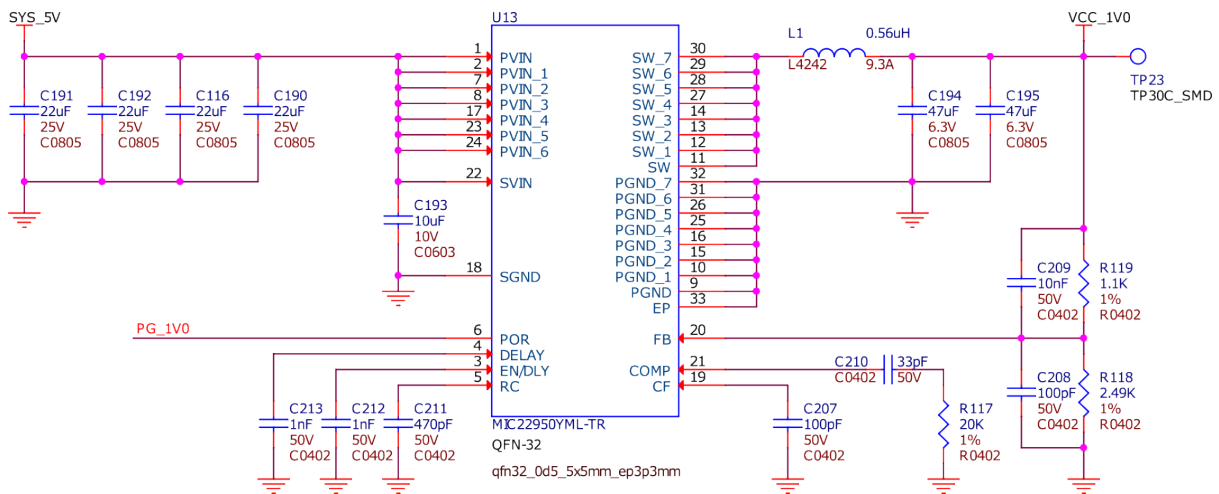


Fig. 3.12: VCC 1V0

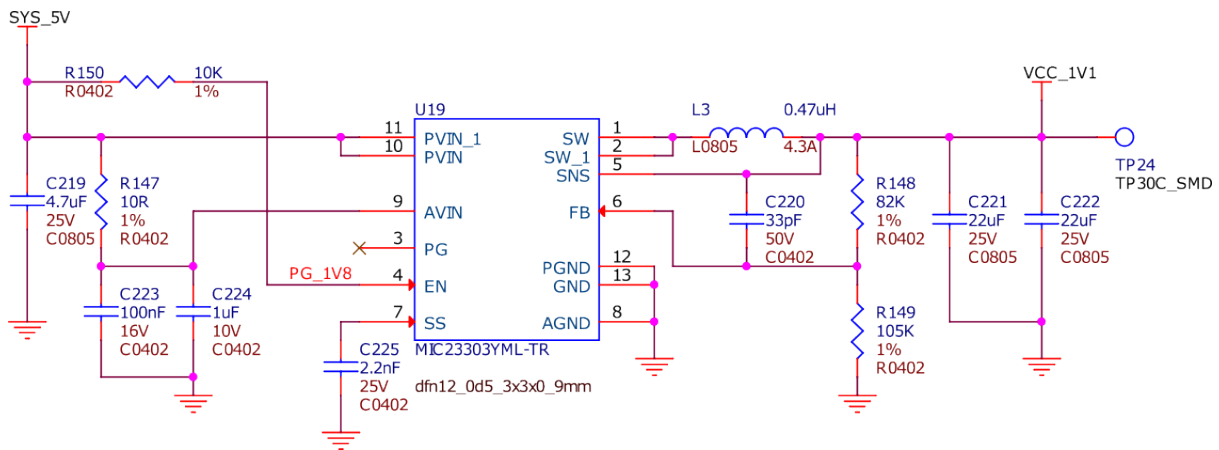


Fig. 3.13: VCC 1V1

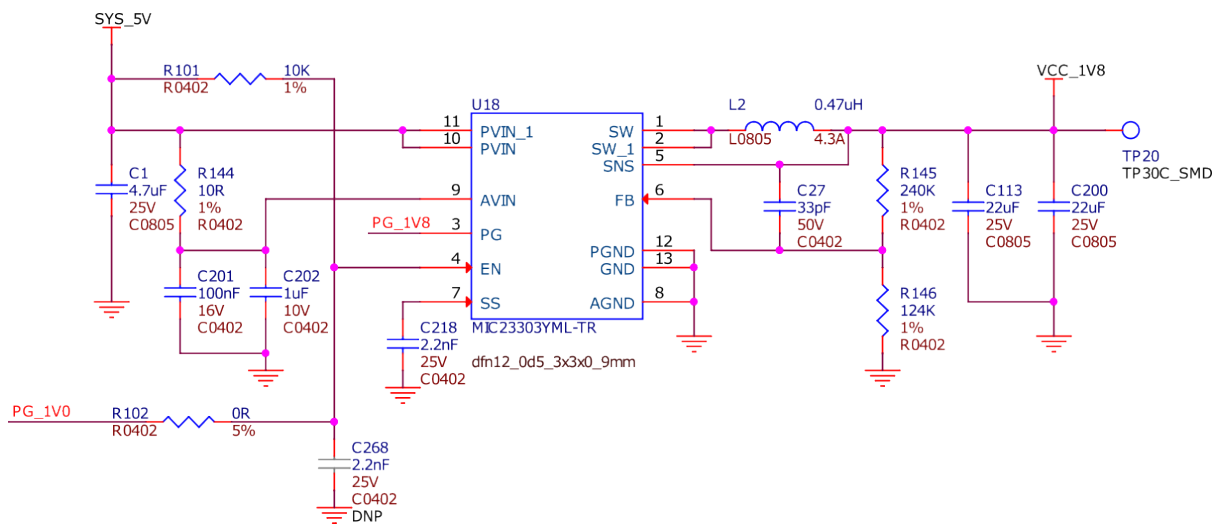


Fig. 3.14: VCC 1V8

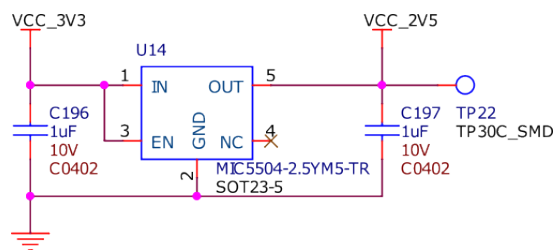


Fig. 3.15: VCC 2V5

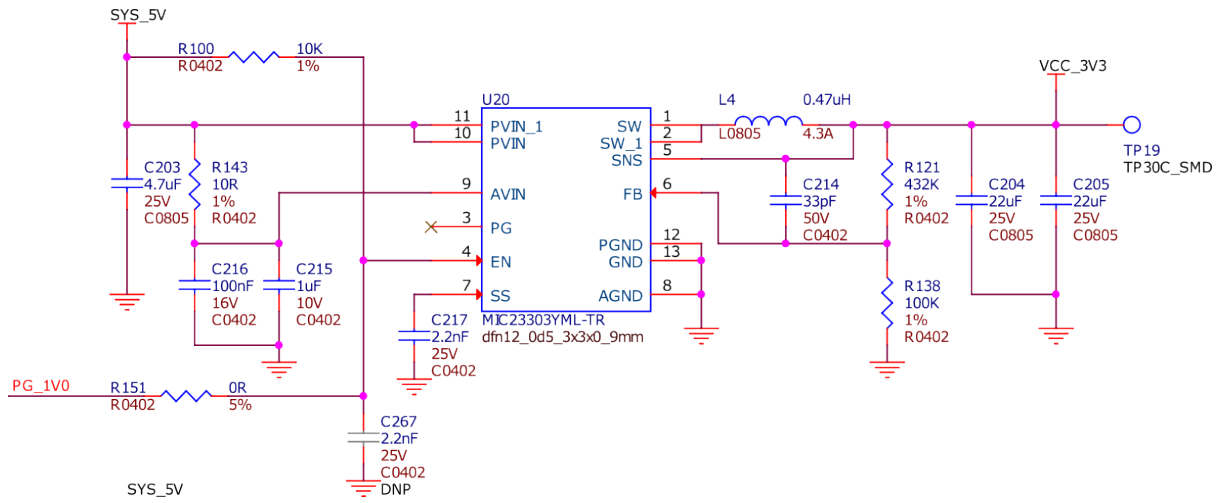


Fig. 3.16: VCC 3V3

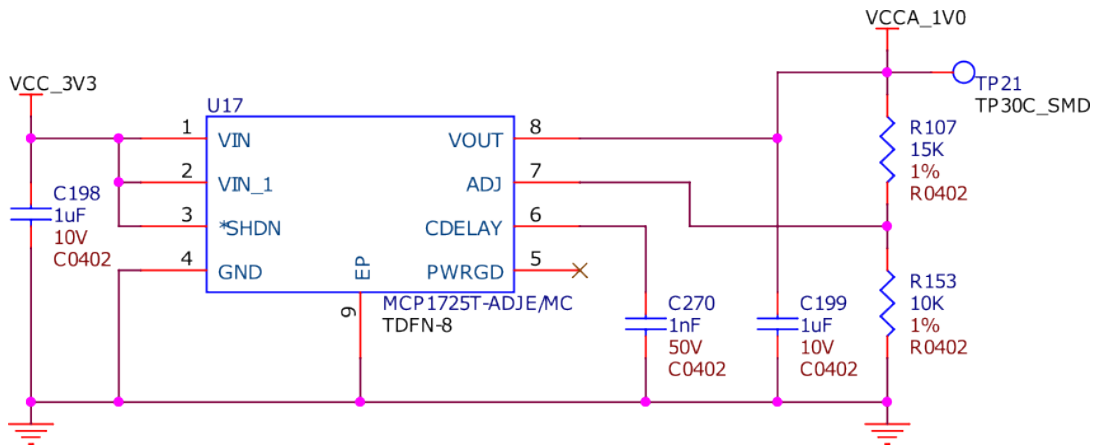


Fig. 3.17: VCCA 1V0

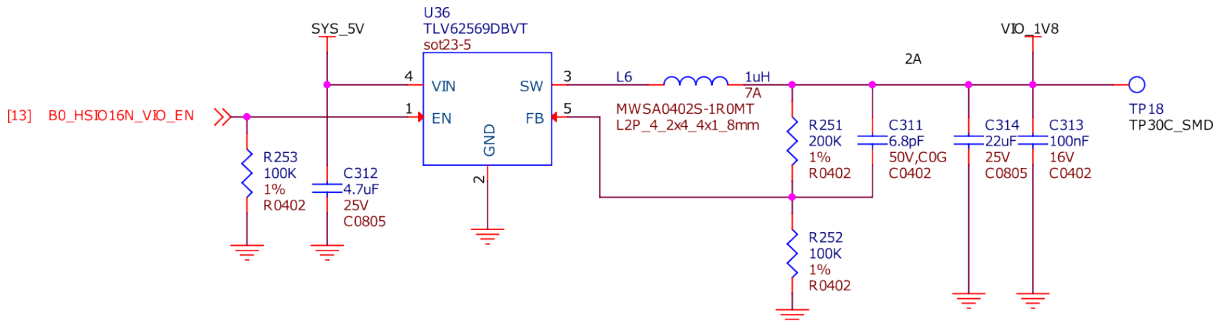


Fig. 3.18: VIO enable





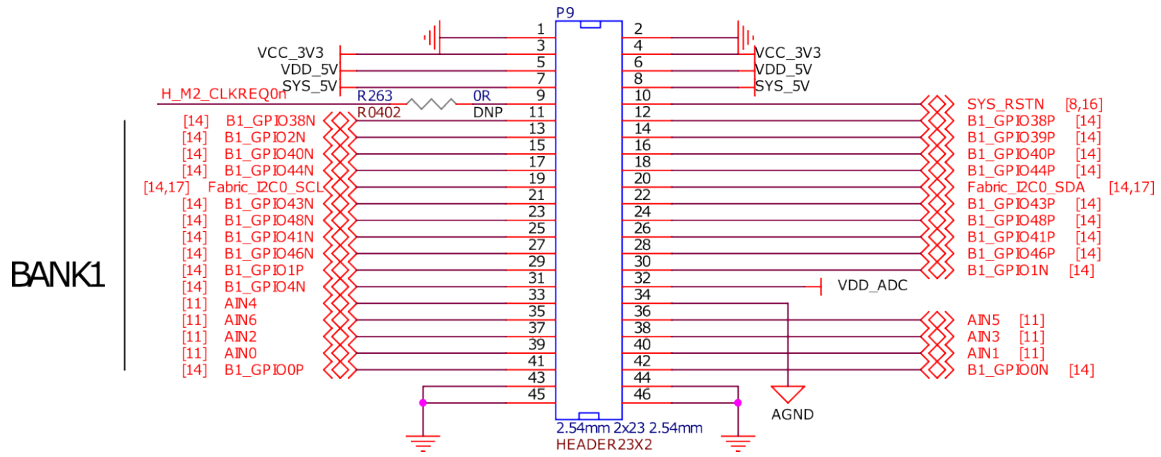


Fig. 3.21: P9 cape header

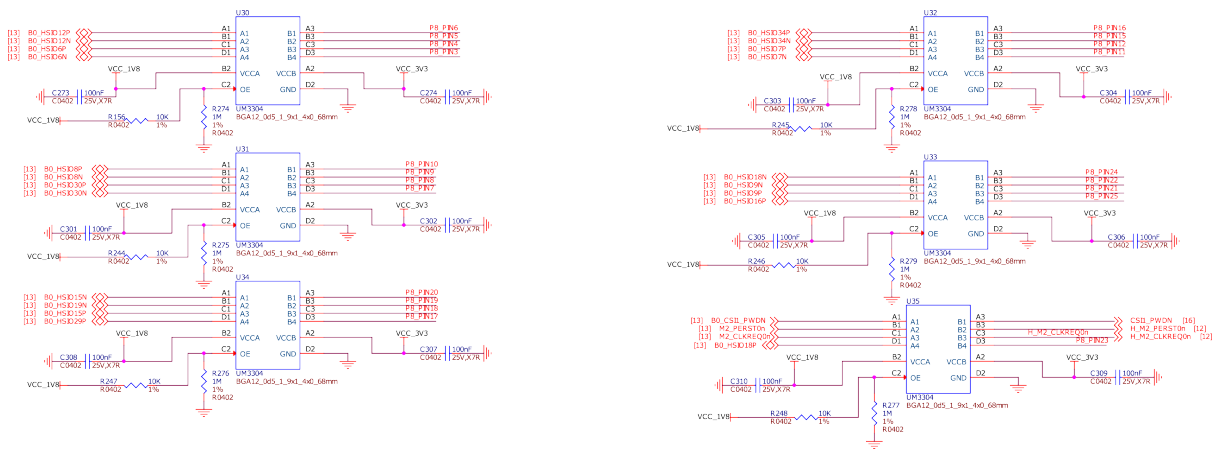


Fig. 3.22: Cape header voltage level translator

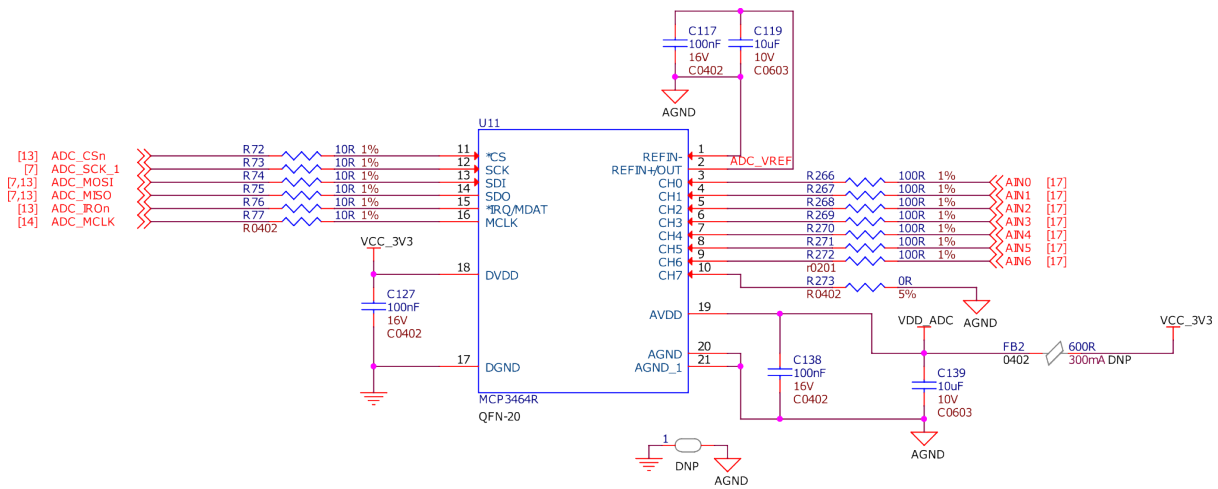


Fig. 3.23: 16bit Delta-Sigma ADC

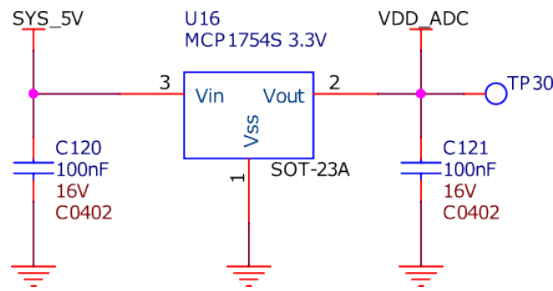


Fig. 3.24: ADC LDO power supply

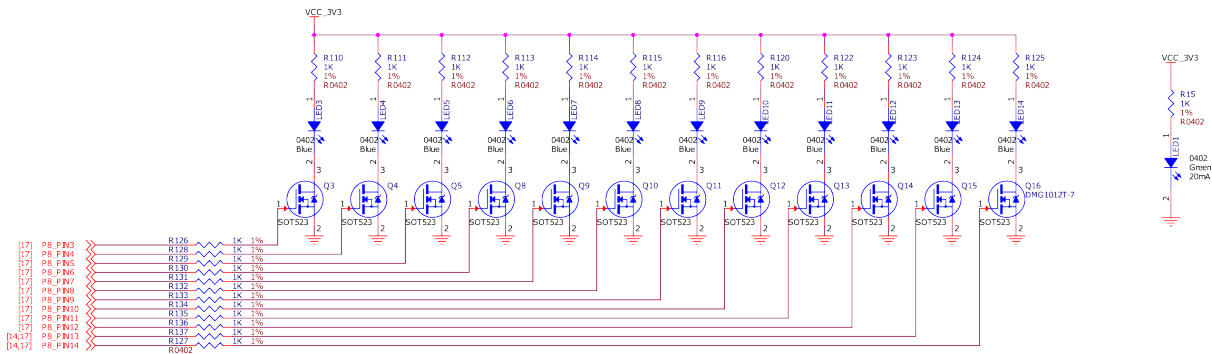


Fig. 3.25: User LEDs and power LED

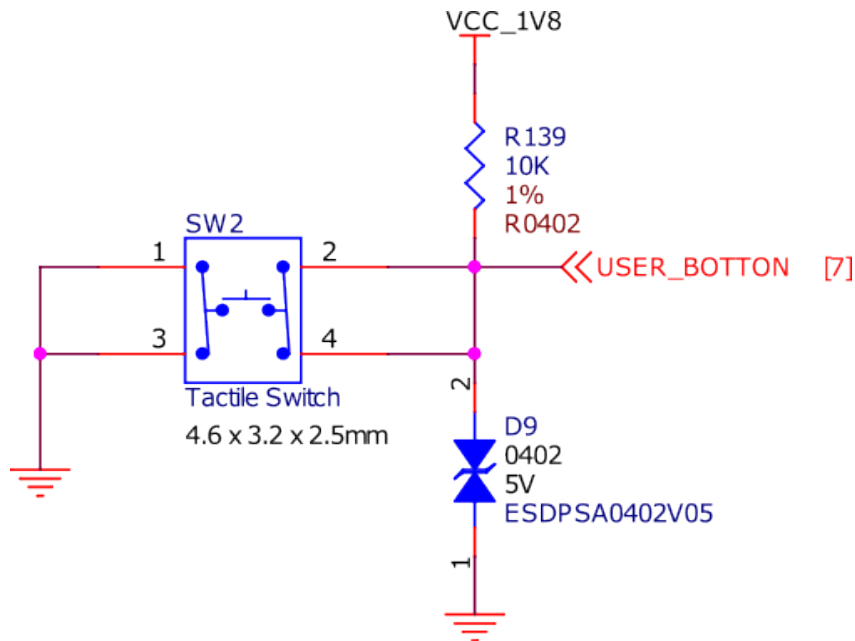


Fig. 3.26: User button

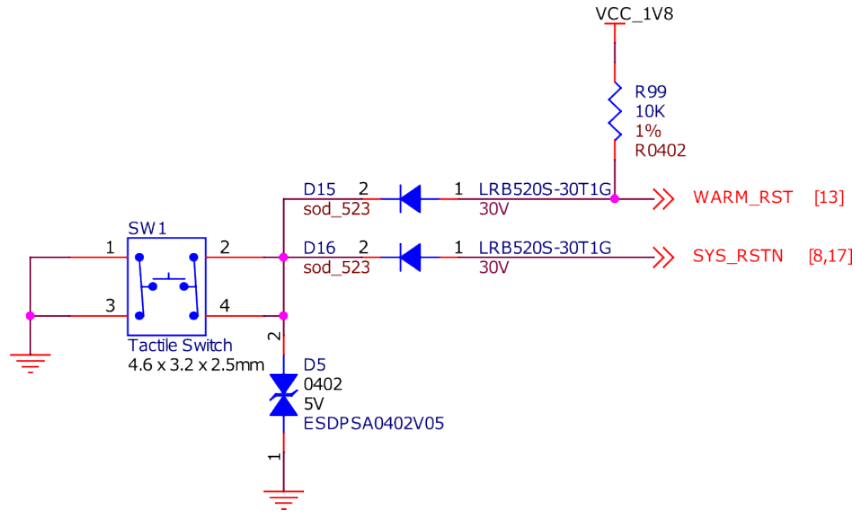


Fig. 3.27: Reset button

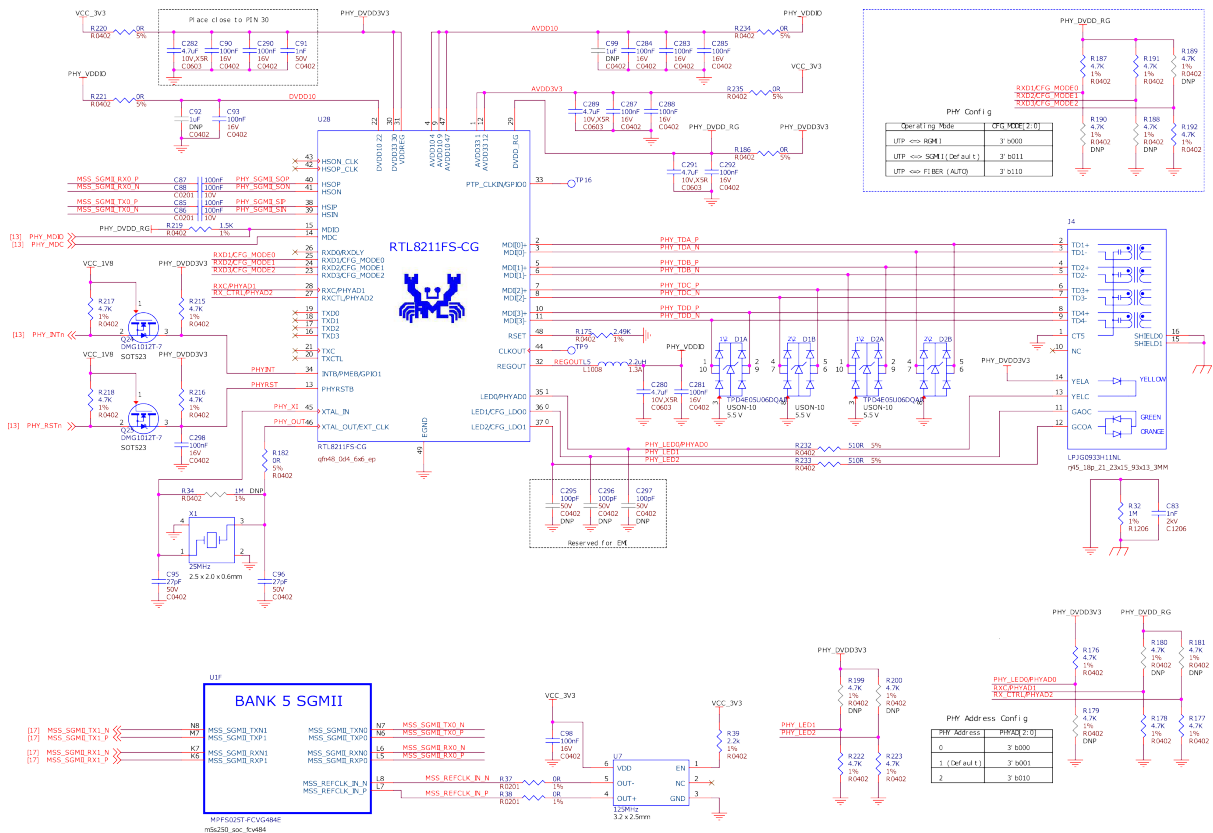


Fig. 3.28: Gigabit ethernet

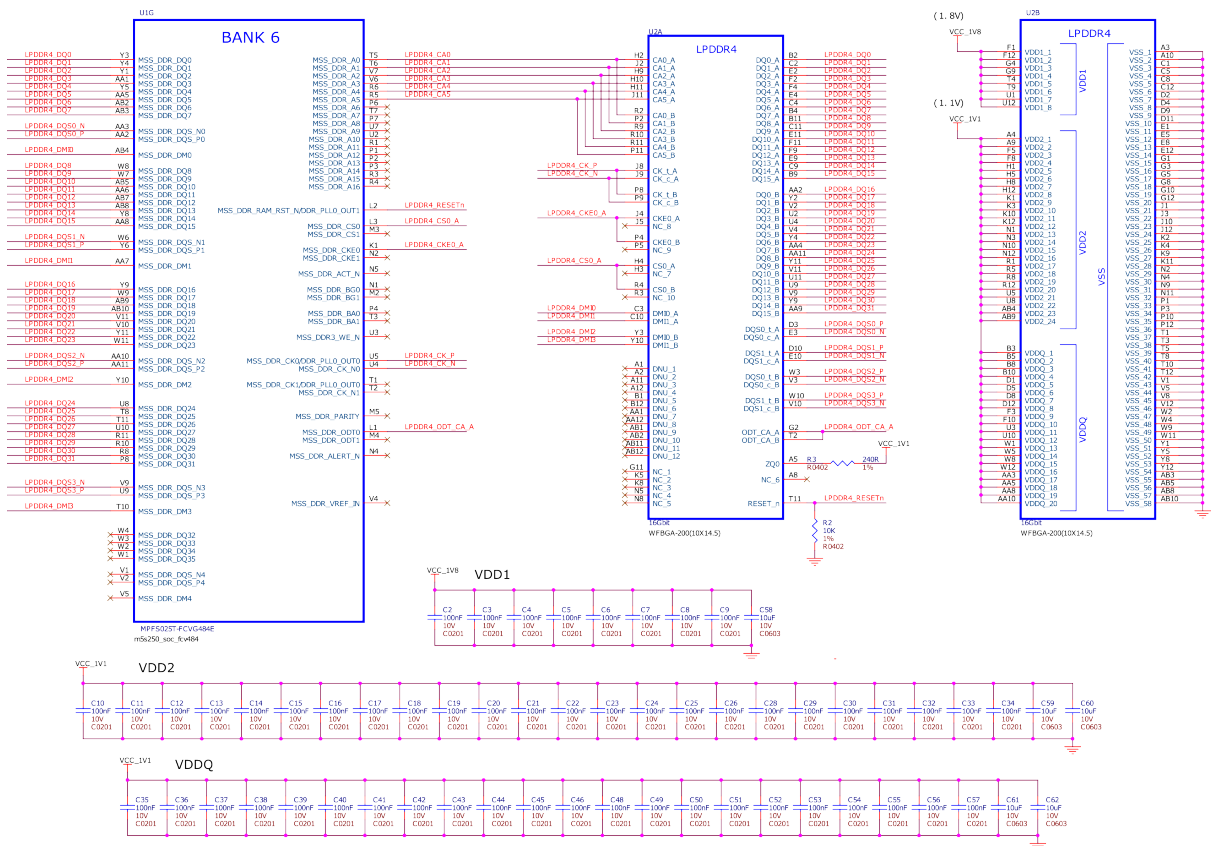


Fig. 3.29: LPDDR memory

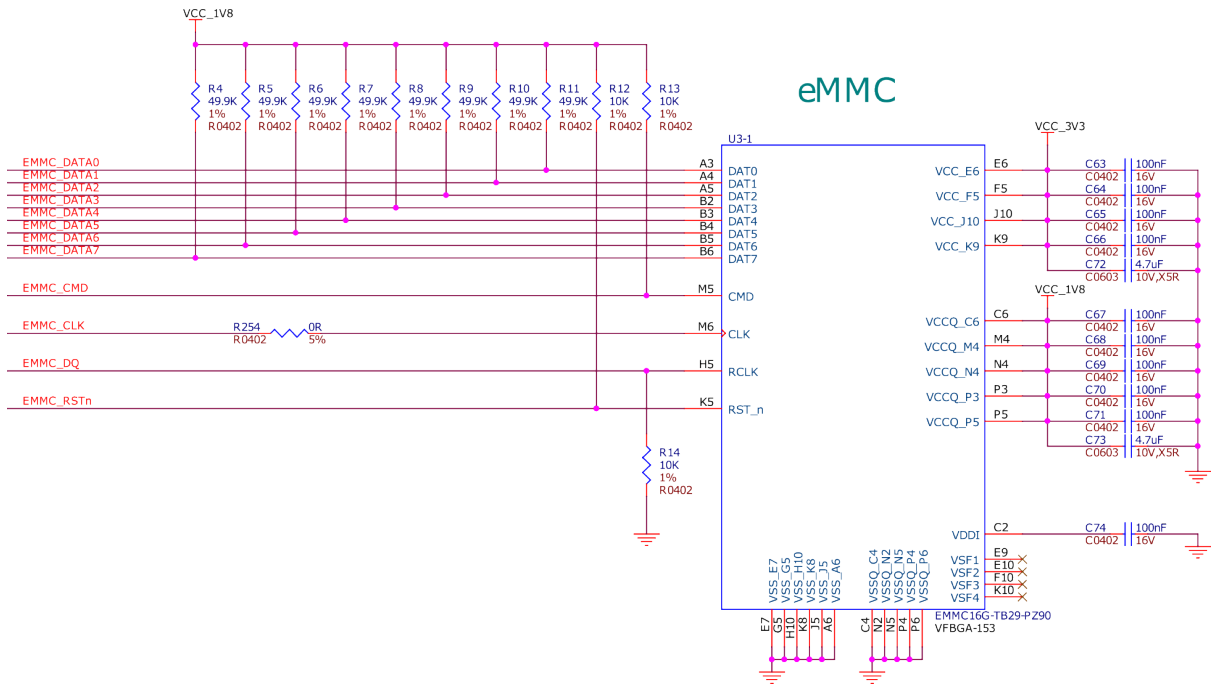


Fig. 3.30: eMMC flash storage

### 3.7.3 microSD

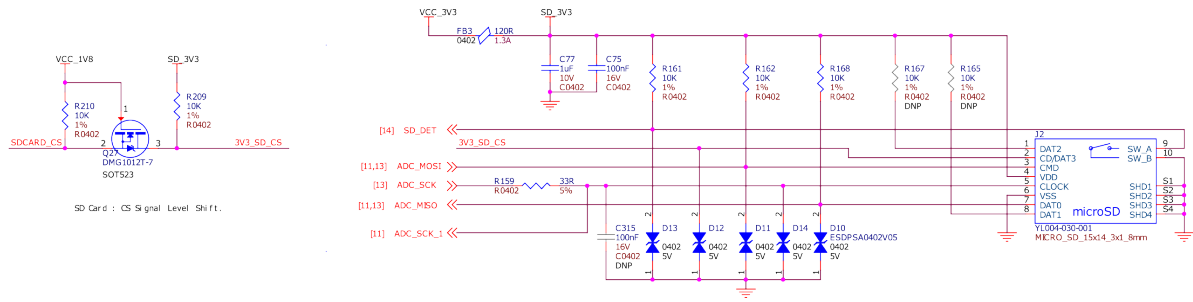


Fig. 3.31: SD Card socket

### 3.7.4 EEPROM

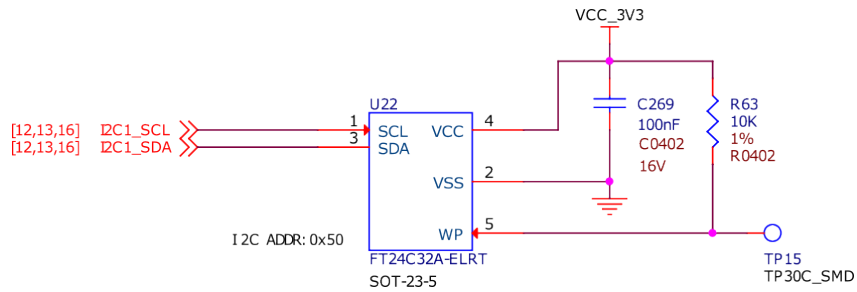


Fig. 3.32: EEPROM

### 3.7.5 SPI flash

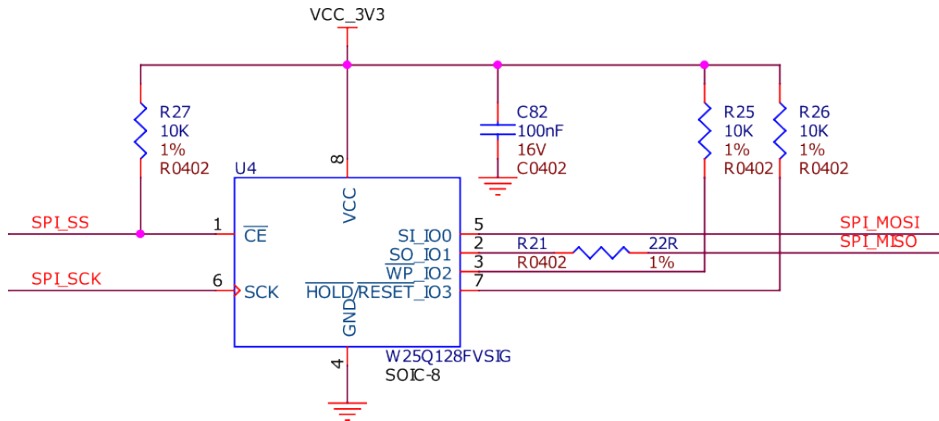


Fig. 3.33: SPI Flash

## 3.8 Multimedia I/O

### 3.8.1 CSI

### 3.9 Debug

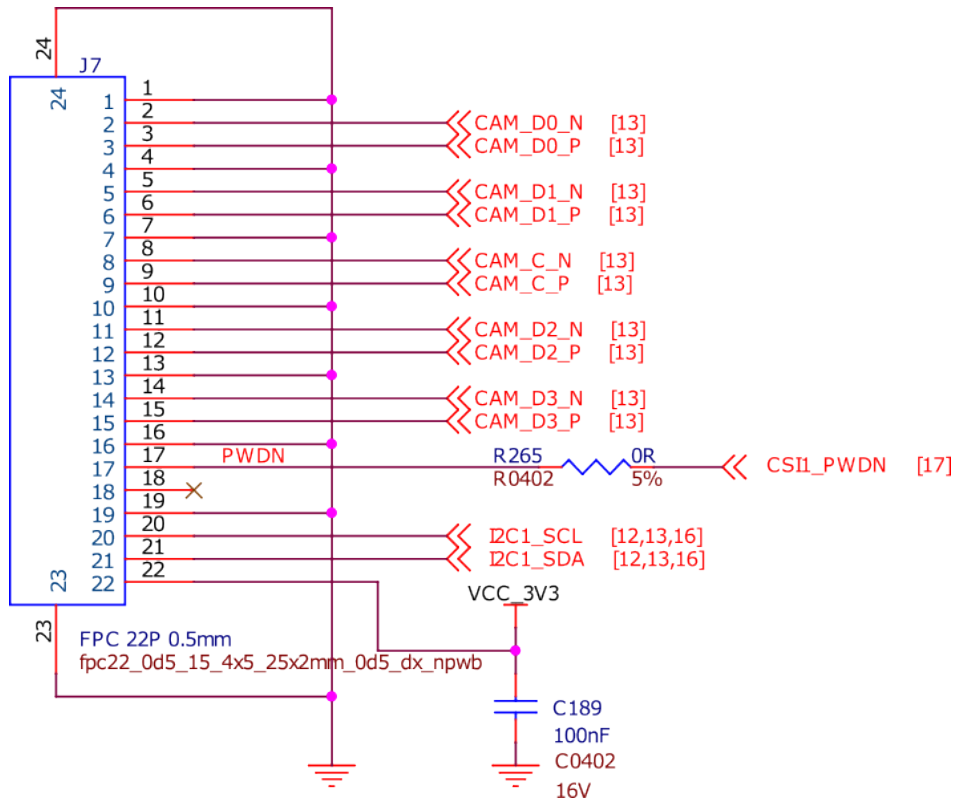


Fig. 3.34: CSI

### 3.9.1 UART debug port

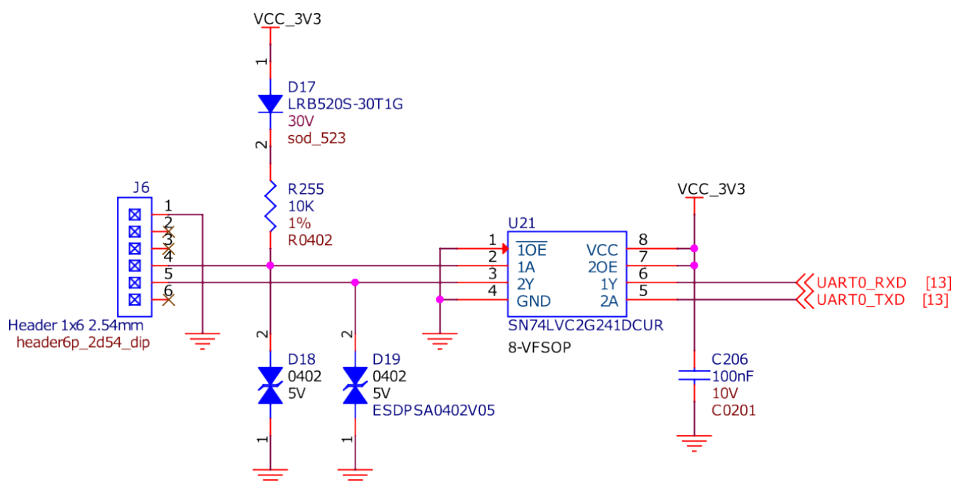


Fig. 3.35: UART debug header

### 3.9.2 JTAG debug port

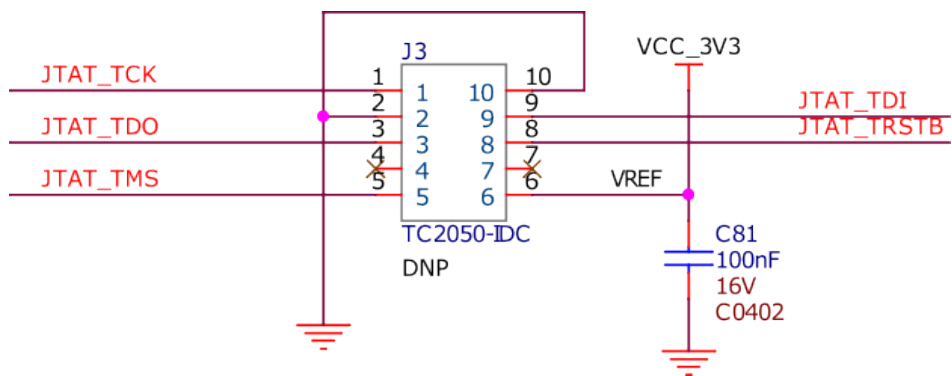


Fig. 3.36: JTAG debug header

### 3.10 Mechanical Specifications

Table 3.1: Dimensions & weight

Parameter	Values
Size	86.38 * 54.61 * 18.8 mm
Max heigh	18.8 mm
PCB Size	86.38 * 54.6 mm
PCB Layers	12 Layers
PCB Thickness	1.6 mm
RoHS compliant	Yes
Gross Weight	106 g
Net weight	45.8 g

# Chapter 4

## Expansion

### 4.1 Cape Headers

---

**Important:** This page is a work in progress, don't use it for debugging.

---

The expansion interface on the board is comprised of two headers P8 (46 pin) & P9 (46 pin). All signals on the expansion headers are **3.3V** unless otherwise indicated.

---

**Note:** Do not connect 5V logic level signals to these pins or the board will be damaged.

---

---

**Note:** DO NOT APPLY VOLTAGE TO ANY I/O PIN WHEN POWER IS NOT SUPPLIED TO THE BOARD. IT WILL DAMAGE THE PROCESSOR AND VOID THE WARRANTY.

---

**NO PINS ARE TO BE DRIVEN UNTIL AFTER THE SYS\_RESET LINE GOES HIGH.**

#### 4.1.1 Connector P8

The following tables show the pinout of the **P8** expansion header. The gateway image is responsible for setting the function of each pin. Refer to the processor documentation for more information on these pins and detailed descriptions of all of the pins listed. In some cases there may not be enough signals to complete a group of signals that may be required to implement a total interface.

The column heading is the pin number on the expansion header.

The **Name** row is the pin name on the processor.

The **BALL** row is the pin number on the processor.

The rows below **BALL** are the gateway setting for each pin.

**NOTES:**

**DO NOT APPLY VOLTAGE TO ANY I/O PIN WHEN POWER IS NOT SUPPLIED TO THE BOARD. IT WILL DAMAGE THE PROCESSOR AND VOID THE WARRANTY.**

**NO PINS ARE TO BE DRIVEN UNTIL AFTER THE SYS\_RESET LINE GOES HIGH.**



**P8.01-P8.02**

P8.01	P8.02
GND	GND

**P8.03-P8.05**

Pin	P8.03	P8.04	P8.05
Name	HSIO6NB0	HSIO6PB0/CCC_NE_CLKIN_N_11	HSIO12NB0
BALL	V22	W22	V19
DEFAULT	MSS GPIO_2[0] User LED 0	MSS GPIO_2[1] User LED 1	MSS GPIO_2[2] User LED 2
GPIOs	MSS GPIO_2[0] User LED 0	MSS GPIO_2[1] User LED 1	MSS GPIO_2[2] User LED 2
ROBOTICS	MSS GPIO_2[0] User LED 0	MSS GPIO_2[1] User LED 1	MSS GPIO_2[2] User LED 2

**P8.06-P8.09**

Pin	P8.06	P8.07	P8.08	P8.09
Name	HSIO12PB0/CLKIN_N_9/CCC_NE_CLKIN_N_9	HSIO30NB0	HSIO30PB0/CLKIN_N_3/CCC_NW_CLKIN_N_3	HSIO8NB0
BALL	V20	V15	V14	V21
DEFAULT	MSS GPIO_2[3] User LED 3	MSS GPIO_2[4] User LED 4	MSS GPIO_2[5] User LED 5	MSS GPIO_2[6] User LED 6
GPIOs	MSS GPIO_2[3] User LED 3	MSS GPIO_2[4] User LED 4	MSS GPIO_2[5] User LED 5	MSS GPIO_2[6] User LED 6
ROBOTICS	MSS GPIO_2[3] User LED 3	MSS GPIO_2[4] User LED 4	MSS GPIO_2[5] User LED 5	MSS GPIO_2[6] User LED 6

**P8.10-P8.13**

Pin	P8.10	P8.11	P8.12	P8.13
Name	HSIO8PB0/CCC_NE_CLKIN_N_10/CCC_NE_PLL0_OUT	HSIO7NB0	HSIO7PB0/CCC_NE_PLL0_OUT	GPIO47PB1
BALL	W21	Y21	Y20	B10
DEFAULT	MSS GPIO_2[7] User LED 7	MSS GPIO_2[8] User LED 8	MSS GPIO_2[9] User LED 9	core_pwm[1] @ 0x41500000 PWM_2:1
GPIOs	MSS GPIO_2[7] User LED 7	MSS GPIO_2[8] User LED 8	MSS GPIO_2[9] User LED 9	MSS GPIO_2[10] User LED 10
ROBOTICS	MSS GPIO_2[7] User LED 7	MSS GPIO_2[8] User LED 8	MSS GPIO_2[9] User LED 9	core_pwm[1] @ 0x41500000 PWM_2:1

**P8.14-P8.16**

Pin	P8.14	P8.15	P8.16
Name	GPIO47NB1	HSIO34NB0	HSIO34PB0/CCC_NW_CLKIN_N_1
BALL	B9	T12	U12
DEFAULT	MSS GPIO_2[11] User LED 11	MSS GPIO_2[12] GPIO	MSS GPIO_2[13] GPIO
GPIOs	MSS GPIO_2[11] User LED 11	MSS GPIO_2[12] GPIO	MSS GPIO_2[13] GPIO
ROBOTICS	MSS GPIO_2[11] User LED 11	MSS GPIO_2[12] GPIO	MSS GPIO_2[13] GPIO

**P8.17-P8.19**

Pin	P8.17	P8.18	P8.19
Name	HSIO29PB0	HSIO15PB0/DQS/CCC_NE_PLL1_OUT0	HSIO19NB0
BALL	W13	T16	W18
DEFAULT	MSS GPIO_2[14] GPIO	MSS GPIO_2[15] GPIO	core_pwm[0] @ 0x41500000 PWM_2:0
GPIOs	MSS GPIO_2[14] GPIO	MSS GPIO_2[15] GPIO	MSS GPIO_2[16] GPIO
ROBOTICS	MSS GPIO_2[14] GPIO	MSS GPIO_2[15] GPIO	core_pwm[0] @ 0x41500000 PWM_2:0

**P8.20-P8.22**

Pin	P8.20	P8.21	P8.22
Name	HSIO15NB0/DQS	HSIO9PB0/DQS/CCC_NE_PLL0_OUT0	HSIO9NB0/DQS
BALL	R16	AA21	AA22
DEFAULT	MSS GPIO_2[17] GPIO	MSS GPIO_2[18] GPIO	MSS GPIO_2[19] GPIO
GPIOs	MSS GPIO_2[17] GPIO	MSS GPIO_2[18] GPIO	MSS GPIO_2[19] GPIO
ROBOTICS	MSS GPIO_2[17] GPIO	MSS GPIO_2[18] GPIO	MSS GPIO_2[19] GPIO

**P8.23-P8.26**

Pin	P8.23	P8.24	P8.25	P8.26
Name	HSIO18PB0/CLKIN_N_7	HSIO18NB0	HSIO16PB0	GPIO49NB1
BALL	AB18	AA18	V17	A12
DEFAULT	MSS GPIO_2[20] GPIO	MSS GPIO_2[21] GPIO	MSS GPIO_2[22] GPIO	MSS GPIO_2[23] GPIO
GPIOs	MSS GPIO_2[20] GPIO	MSS GPIO_2[21] GPIO	MSS GPIO_2[22] GPIO	MSS GPIO_2[23] GPIO
ROBOTICS	MSS GPIO_2[20] GPIO	MSS GPIO_2[21] GPIO	MSS GPIO_2[22] GPIO	MSS GPIO_2[23] GPIO

**P8.27-P8.29**

Pin	P8.27	P8.28	P8.29
Name	GPIO49PB1/CLKIN_S_5	GPIO51NB1	GPIO51PB1/CLKIN_S_6
BALL	A13	B14	B13
DEFAULT	MSS GPIO_2[24] GPIO	MSS GPIO_2[25] GPIO	MSS GPIO_2[26] GPIO
GPIOs	MSS GPIO_2[24] GPIO	MSS GPIO_2[25] GPIO	MSS GPIO_2[26] GPIO
ROBOTICS	MSS GPIO_2[24] GPIO	MSS GPIO_2[25] GPIO	MSS GPIO_2[26] GPIO

**P8.30-P8.32**

Pin	P8.30	P8.31	P8.32
Name	GPIO50NB1/DQS	GPIO50PB1/DQS	GPIO53NB1
BALL	D14	D13	B15
DEFAULT	MSS GPIO_2[27] GPIO	core_gpio[0] @ 0x41100000 GPIO	core_gpio[1] @ 0x41100000 GPIO
GPIOs	MSS GPIO_2[27] GPIO	core_gpio[0] @ 0x41100000 GPIO	core_gpio[1] @ 0x41100000 GPIO
ROBOTICS	MSS GPIO_2[27] GPIO	core_gpio[0] @ 0x41100000 GPIO	core_gpio[1] @ 0x41100000 GPIO

**P8.33-P8.35**

Pin	P8.33	P8.34	P8.35
Name	GPIO53PB1/CLKIN_S_7	GPIO52NB1/LPRB_B	GPIO52PB1/LPRB_A
BALL	A15	C15	C14
DEFAULT	core_gpio[2] @ 0x41100000 GPIO	core_gpio[3] @ 0x41100000 GPIO	core_gpio[4] @ 0x41100000 GPIO
GPIOs	core_gpio[2] @ 0x41100000 GPIO	core_gpio[3] @ 0x41100000 GPIO	core_gpio[4] @ 0x41100000 GPIO
ROBOTICS	core_gpio[2] @ 0x41100000 GPIO	core_gpio[3] @ 0x41100000 GPIO	core_gpio[4] @ 0x41100000 GPIO

**P8.36-P8.38**

Pin	P8.36	P8.37	P8.38
Name	GPIO37NB1	GPIO37PB1/CCC_SW_CLKIN_S_1	GPIO3NB1
BALL	B4	C4	C17
DEFAULT	core_gpio[5] @ 0x41100000 GPIO	core_gpio[6] @ 0x41100000 GPIO	core_gpio[7] @ 0x41100000 GPIO
GPIOs	core_gpio[5] @ 0x41100000 GPIO	core_gpio[6] @ 0x41100000 GPIO	core_gpio[7] @ 0x41100000 GPIO
ROBOTICS	core_gpio[5] @ 0x41100000 GPIO	core_gpio[6] @ 0x41100000 GPIO	core_gpio[7] @ 0x41100000 GPIO

**P8.39-P8.41**

Pin	P8.39	P8.40	P8.41
Name	GPIO3PB1/CCC_SE_CLKIN_S_10/CCC_SE_PLL1_OUT0	GPIO5NB1	GPIO5PB1/CCC_SE_CLKIN_S_11
BALL	B17	B18	A18
DEFAULT	core_gpio[8] @ 0x41100000 GPIO	core_gpio[9] @ 0x41100000 GPIO	core_gpio[10] @ 0x41100000 GPIO
GPIOs	core_gpio[8] @ 0x41100000 GPIO	core_gpio[9] @ 0x41100000 GPIO	core_gpio[10] @ 0x41100000 GPIO
ROBOTICS	core_gpio[8] @ 0x41100000 GPIO	core_gpio[9] @ 0x41100000 GPIO	core_gpio[10] @ 0x41100000 GPIO

**P8.42-P8.44**

Pin	P8.42	P8.43	P8.44
Name	GPIO36NB1	GPIO36PB1/CCC_SW_CLKIN_S_0	GPIO42NB1
BALL	D6	D7	D8
DEFAULT	core_gpio[11] @ 0x41100000 GPIO	core_gpio[12] @ 0x41100000 GPIO	core_gpio[13] @ 0x41100000 GPIO
GPIOs	core_gpio[11] @ 0x41100000 GPIO	core_gpio[12] @ 0x41100000 GPIO	core_gpio[13] @ 0x41100000 GPIO
ROBOTICS	core_gpio[11] @ 0x41100000 GPIO	core_gpio[12] @ 0x41100000 GPIO	core_gpio[13] @ 0x41100000 GPIO

**P8.45-P8.46**

Pin	P8.45	P8.46
Name	GPIO42PB1	GPIO4PB1/CCC_SE_PLL1_OUT1
BALL	D9	D18
DEFAULT	core_gpio[14] @ 0x41100000 GPIO	core_gpio[15] @ 0x41100000 GPIO
GPIOs	core_gpio[14] @ 0x41100000 GPIO	core_gpio[15] @ 0x41100000 GPIO
ROBOTICS	core_gpio[14] @ 0x41100000 GPIO	core_gpio[15] @ 0x41100000 GPIO

**4.1.2 Connector P9**

The following tables show the pinout of the **P9** expansion header. The gateway image is responsible for setting the function of each pin. Refer to the processor documentation for more information on these pins and detailed descriptions of all of the pins listed. In some cases there may not be enough signals to complete a group of signals that may be required to implement a total interface.

The column heading is the pin number on the expansion header.

The **Name** row is the pin name on the processor.

The **BALL** row is the pin number on the processor.

The rows below **BALL** are the gateway setting for each pin.

**NOTES:**

**DO NOT APPLY VOLTAGE TO ANY I/O PIN WHEN POWER IS NOT SUPPLIED TO THE BOARD. IT WILL DAMAGE THE PROCESSOR AND VOID THE WARRANTY.**

**NO PINS ARE TO BE DRIVEN UNTIL AFTER THE SYS\_RESET LINE GOES HIGH.**

**P9.01-P9.05**

P9.01	P9.02	P9.03	P9.04	P9.05
GND	GND	VCC_3V3	VCC_3V3	VDD_5V

**P9.06-P9.10**

P9.06	P9.07	P9.08	P9.10
VDD_5V	SYS_5V	SYS_5V	SYS_RSTN

Pin	P9.09
Name	HSIO19PB0
BALL	W19

**P9.11-P9.13**

Pin	P9.11	P9.12	P9.13
Name	GPIO38NB1/DQS	GPIO38PB1/DQS/CCC_SW_PLL1_OUT0	GPIO2NB1/DQS
BALL	B5	C5	D19
DEFAULT	MMUART4	core_gpio[1] @ 0x41200000	MMUART4
	UART4 RX	GPIO	UART4 TX
GPIOs	core_gpio[0] @ 0x41200000	core_gpio[1] @ 0x41200000	core_gpio[2] @ 0x41200000
	GPIO	GPIO	GPIO
ROBOTICS	~	core_gpio[0] @ 0x41200000	core_gpio[7] @ 0x41200000
	~	GPIO	GPIO

**P9.14-P9.16**

Pin	P9.14	P9.15	P9.16
Name	GPIO39PB1/CLKIN_S_2/CCC_SW_CLKIN_S_2/CCC_SW_PLL1_O	GPIO40NB1	GPIO40PB1/CCC_SW_PLL1_OUT1
BALL	C6	A5	A6
DEFAULT	core_pwm[0] @ 0x41400000	core_gpio[4] @ 0x41200000	@ core_pwm[1] @ 0x41400000
	PWM_1:0	GPIO	PWM_1:1
GPIOs	core_gpio[3] @ 0x41200000	core_gpio[4] @ 0x41200000	@ core_gpio[5] @ 0x41200000
	GPIO	GPIO	GPIO
ROBOTICS	core_pwm[0] @ 0x41400000	core_gpio[1] @ 0x41200000	@ core_pwm[1] @ 0x41400000
	PWM_1:0	GPIO	PWM_1:1

**P9.17-P9.19**

Pin	P9.17	P9.18	P9.19
Name	GPIO44NB1/DQS	GPIO44PB1/DQS/CCC_SW_PLLO_OUT0	GPIO45PB1/CCC_SW_PLLO_OUT0
BALL	C9	C10	A10
DEFAULT	~	~	MSS I2C0
	~	~	I2C0 SCL
GPIOs	core_gpio[6] @ 0x41200000	core_gpio[7] @ 0x41200000	MSS I2C0
	GPIO	GPIO	I2C0 SCL
ROBOTICS	~	~	MSS I2C0
	~	~	I2C0 SCL

**P9.20-P9.22**

Pin	P9.20	P9.21	P9.22
Name	GPIO45NB1	GPIO43NB1	GPIO43PB1
BALL	A11	B8	A8
DEFAULT	MSS I2C0	~	~
	I2C0 SDA	~	~
GPIOs	MSS I2C0	core_gpio[8] @ 0x41200000	core_gpio[8] @ 0x41200000
	I2C0 SDA	GPIO	GPIO
ROBOTICS	MSS I2C0	~	~
	I2C0 SDA	~	~

**P9.23-P9.25**

Pin	P9.23	P9.24	P9.25
Name	GPIO48NB1	GPIO48PB1/CLKIN_S_4	GPIO41NB1
BALL	C12	B12	B7
DEFAULT	core_gpio[10] @ 0x41200000	~	core_gpio[12] @ 0x41200000
	GPIO	~	GPIO
GPIOs	core_gpio[10] @ 0x41200000	core_gpio[11] @ 0x41200000	core_gpio[12] @ 0x41200000
	GPIO	GPIO	GPIO
ROBOTICS	core_gpio[2] @ 0x41200000	~	core_gpio[3] @ 0x41200000
	GPIO	~	GPIO

**P9.26-P9.28**

Pin	P9.26	P9.27	P9.28
Name	GPIO41PB1/CLKIN_S_3/CCC_SW_CLKIN_S_3	GPIO46NB1	GPIO46PB1/CCC_SW_PLL0_OUT1
BALL	A7	D11	C11
DEFAULT	~	core_gpio[14] @ 0x41200000	~
	~	GPIO	~
GPIOs	core_gpio[13] @ 0x41200000	core_gpio[14] @ 0x41200000	core_gpio[15] @ 0x41200000
	GPIO	GPIO	GPIO
ROBOTICS	~	~	~
	~	~	~

**P9.29-P9.31**

Pin	P9.29	P9.30	P9.31
Name	GPIO1PB1/CLKIN_S_9/CCC_SE_CLKIN_S_9	GPIO1NB1	GPIO4NB1
BALL	F17	F16	E18
DEFAULT	~	core_gpio[17] @ 0x41200000	~
	~	GPIO	~
GPIOs	core_gpio[16] @ 0x41200000	core_gpio[17] @ 0x41200000	core_gpio[18] @ 0x41200000
	GPIO	GPIO	GPIO
ROBOTICS	~	core_gpio[5] @ 0x41200000	~
	~	GPIO	~

**P9.32-P9.40**

P9.32	P9.34
VDD_ADC	GND

P9.33	P9.35	P9.36	P9.37	P9.38	P9.39	P9.40
AIN4	AIN6	AIN5	AIN2	AIN3	AIN0	AIN1

### P9.41-P9.42

Pin	P9.41	P9.42
Name	GPIO0PB1/CLKIN_S_8/CCC_SE_CLKIN_S_8/CCC_SE_PLL0_OUT0	GPIO0NB1
BALL	E15	E14
DEFAULT	core_gpio[19] @ 0x41200000 GPIO	core_pwm[0] @ 0x41000000 PWM_0:0
GPIOs	core_gpio[19] @ 0x41200000 GPIO	core_gpio[20] @ 0x41200000 GPIO
ROBOTICS	core_gpio[19] @ 0x41200000 GPIO	~ ~

### P9.43-P9.46

P9.43	P9.44	P9.45	P9.46
GND	GND	GND	GND

# Chapter 5

## Demos

---

**Todo:** We need a CSI capture demos

---

---

**Todo:** We need a cape compatibility layer demo

---

### 5.1 Upgrade BeagleV-Fire Gateway

This document describes how to upgrade your BeagleV-Fire's gateway. This approach can be used out of the box using Linux commands executed on BeagleV-Fire

#### 5.1.1 Required Equipment

- BeagleV-Fire board
- USB-C cable
- Ethernet cable

The USB-C cable provides power, a serial interface to BeagleV-Fire and allows connecting to BeagleV-Fire through a browser using IP address 192.168.7.2.

The Ethernet cable connected to your local network (LAN) allows connecting to BeagleV-Fire using the SSH protocol. It also allows BeagleV-Fire to retrieve updated packages through your local network's Internet connection.

#### 5.1.2 Connect to BeagleV-Fire Linux Command Line Interface

BeagleV-Fire boots Linux out of the box. Like all Beagleboard boards there are several methods to get BeagleV-Fire's Linux command prompt.

- Cockpit
- SSH
- Serial port



### Cockpit

Enter the following URL in your web browser: `https://beaglev.localdomain:9090/`

On first use, click through the security warning. Login using `beagle/temppwd` as user/password. Click on Terminal in the left pane. You now have a Linux command prompt running on your BeagleV-Fire. Next step: enter the commands described in the Gateway Upgrade Linux Commands section of this document.

---

**Note:** You can connect to the Cockpit using the IP address dynamically assigned to your BeagleV-Fire in your local Ethernet network. One method of finding the value of that dynamically assigned IP address is to open a serial terminal through the USB port and use the `ip address` Linux command. Please refer to the USB Serial Port section.

---

### SSH

Like all Beagleboard boards, you can SSH to the board through the USB interface by using IP address 192.168.7.2.

---

**Note:** On Windows, this approach may require some drivers to be updated or installed. Use one of the other approaches if you are not immediately successful with this one. You can circle back later to adjust your Windows installation if required.

---

### Serial Port

A serial port is available through the USB-C port. This serial port becomes available once Linux has booted on BeagleV-Fire. Please wait a couple of minutes after powering up the board before looking for additional serial ports reported by your host computer's operating system. You can then use your favorite serial port terminal tool such as Putty or Screen to access the BeagleV-Fire Linux command prompt.

For example on your Linux host computer:

```
screen /dev/ttyACM0 115200
```

Where `ttyACM0` is an additional serial port that appeared after BeagleV-Fire was connected to your Linux host computer. This serial port can be identified using the `dmesg | grep tty` Linux command which will show the most recent serial port added to the host computer.

On Windows, BeagleV-Fire's serial port number will show in the Windows Device Manager. Use that serial port number in Putty with a speed 115200 baud, no flow-control.

### 5.1.3 Gateway Upgrade Linux Commands

---

**Note:** BeagleV-Fire needs to be connected to the internet through your local network for the commands in this section to work. The connection can be through the Ethernet port or the Wi-Fi module.

---

#### Install bbb.io-gateway

You need to install the `bbb.io-gateway` package. This will allow retrieving the most up-to-date gateway.

```
sudo apt install bbb.io-gateway
```

---

### Retrieve Available Updated Linux packages List

The list will include the latest BeagleV-Fire gateway packages.

```
sudo apt update
```

### Upgrade Linux Packages

This will upgrade the BeagleV-Fire gateway Linux programming files located under `/usr/share/beagleboard/gateway`. Several directories are found in that location, each containing programming files for one individual gateway configuration.

```
sudo apt upgrade
```

### Launch Reprogramming of BeagleV-Fire's FPGA

Change directory to `/usr/share/beagleboard/gateway`. This directory contains a script performing the gateway's reprogramming. It also contains one directory for each of the possible gateway configuration that can be programmed into your BeagleV-Fire. The name of one of these directories is passed as argument to the script to specify which gateway configuration you wish to program your BeagleV-Fire with.

```
cd /usr/share/beagleboard/gateway
. ./change-gateway.sh default
```

---

**Important:** Do not power-off BeagleV-Fire until it has rebooted by itself. The gateway reprogramming may take a couple of minutes.

---

The change-gateway script programs the selected gateway and its associated device tree overlays into the PolarFire SoC System Controllers SPI flash and triggers a software reboot. During the reboot, the Hart Software Services (HSS) will request the PolarFire SoC System Controller to reprogram the FPGA and eNVM. The PolarFire SoC System Controller will reprogram the FPGA if it finds it contains a different design version than the one in the SPI Flash. The board reboots on completion of the FPGA reprogramming.

## 5.2 Flashing gateway and Linux image

---

**Todo:** This is the *hard* way! Special cables and FlashPros are not required when using the firmware we initially ship on the board. This tutorial should be rescripted as how to `_unbrick_` your board. Also, we have other workarounds using software and GPIOs rather than FlashPros. Let's not put this in user's face as *the* experience when it is far more painful than using the `change-gateway.sh` script and "hold BOOT button when applying power" solutions we've created!

---

In this tutorial we are going to learn to flash the gateway image to FPGA and `sdcard.image` to eMMC storage.

---

**Important:** Additional hardware required:

1. FlashPro5/6 programmer
  2. [Tag connect TC2050-IDC-NL 10-Pin No-Legs Cable with Ribbon connector](#)
  3. [TC2050-CLIP-3PACK Retaining CLIP board for TC2050-NL cables](#)
-

### 5.2.1 Programming & Debug tools installation

To flash a gateway image to your BeagleV-Fire board you will require a FlashPro5/6 and FlashPro Express (FPEXpress) tool which comes pre-installed as part of [Liberio SoC Design Suite](#). A standalone FlashPro Express tool is also available with MicroChip's [Programming and Debug Tools](#) package, which we are going to use for this tutorial. Below are the steps to install the software:

1. Download the zip for your operating system from [Programming and Debug Tools](#) page.
2. Unzip the file and in the unzipped folder you will find `launch_installer.sh` and `Program_Debug_v2023.1.bin`.
3. Execute the `launch_installer.sh` script to start the installation procedure.

```
[lorforlinux@fedora Program_Debug_v2023.1_lin] $ ./launch_installer.sh
No additional packages to install for installer usage
Requirement search complete.
See /tmp/check_req_installer608695.log for information.
Launch of installer
Preparing to install
Extracting the JRE from the installer archive...
Unpacking the JRE...
```

---

**Note:** It's recommended to install under `home/user/microchip` for linux users.

---

#### Enabling non-root user to access FlashPro

1. Download `60-openocd.rules`
2. Copy udev rule `sudo cp 60-openocd.rules /etc/udev/rules.d`
3. Trigger udevadm using `sudo udevadm trigger` or reboot the PC for the changes to take effect

### 5.2.2 Flashing gateway image

---

**Note:** content below is valid for beta testers only.

---

#### Launch FPEXpress

1. Download `FlashProExpress.zip` file and unzip, it contains the `*.job` file which we need to create a new project in FPEXpress.
2. Open up a terminal and go to `/home/user/microchip/Program_Debug_v202X.Y/Program_Debug_Tool/bin` which includes FPEXpress tool.
3. Execute `./FPEXpress` in terminal to start FlashPro Express software.

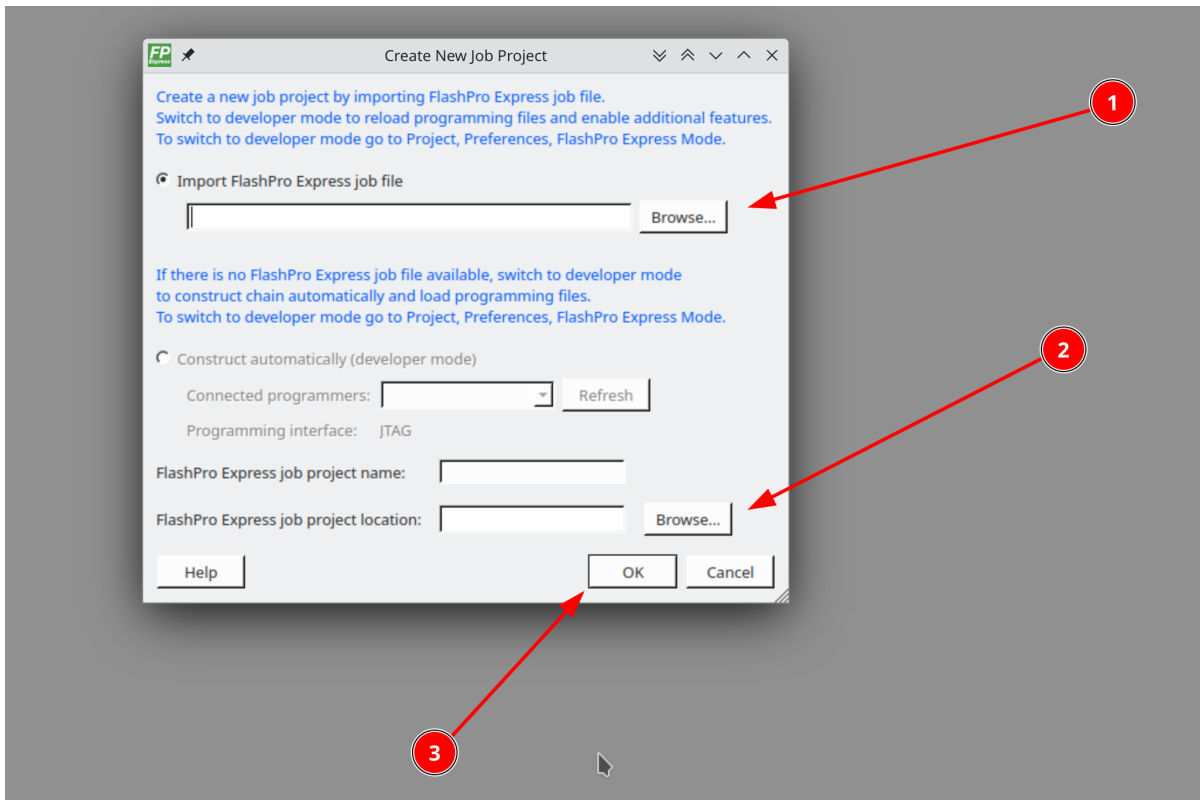
#### Create new project

---

**Important:** Make sure you have your FlashPro5/6 connected before you create a new project.

---

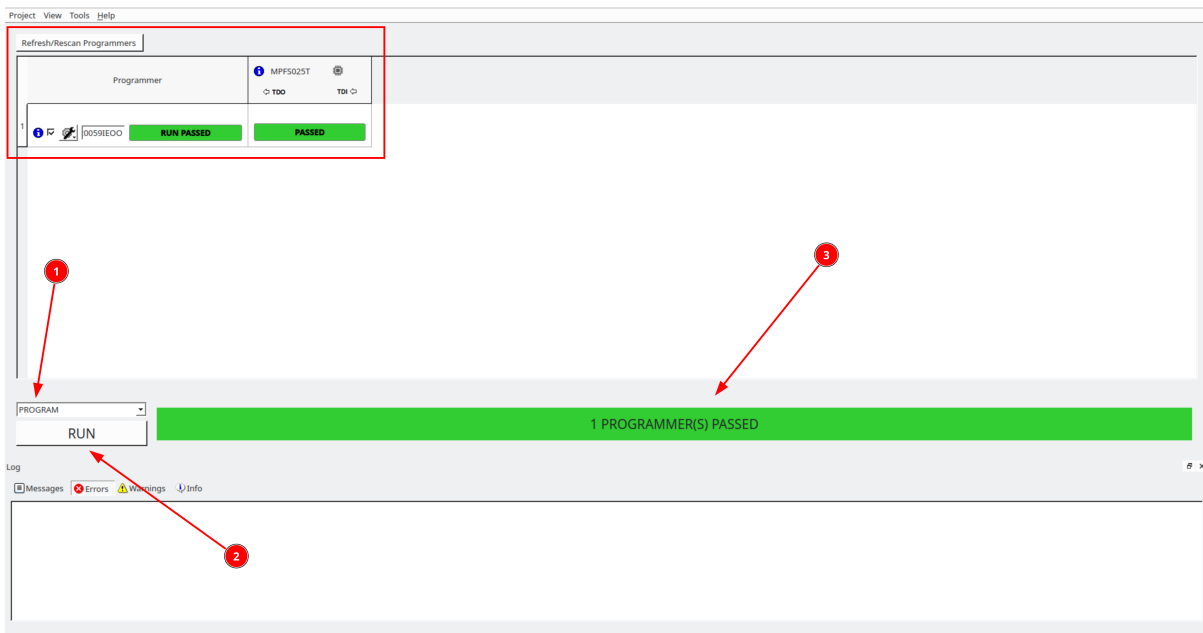
Press CTRL+N to create a file and you will see a pop-up window like shown below,



Follow the steps below as annotated in the image above:

1. Click on browse (1) button to select the job file.
2. Click on browse (2) button to select the project location.
3. Click ok button to finish.

If your FlashPro5/6 is connected properly you'll see the window shown below:



Following the annotation in the image above:

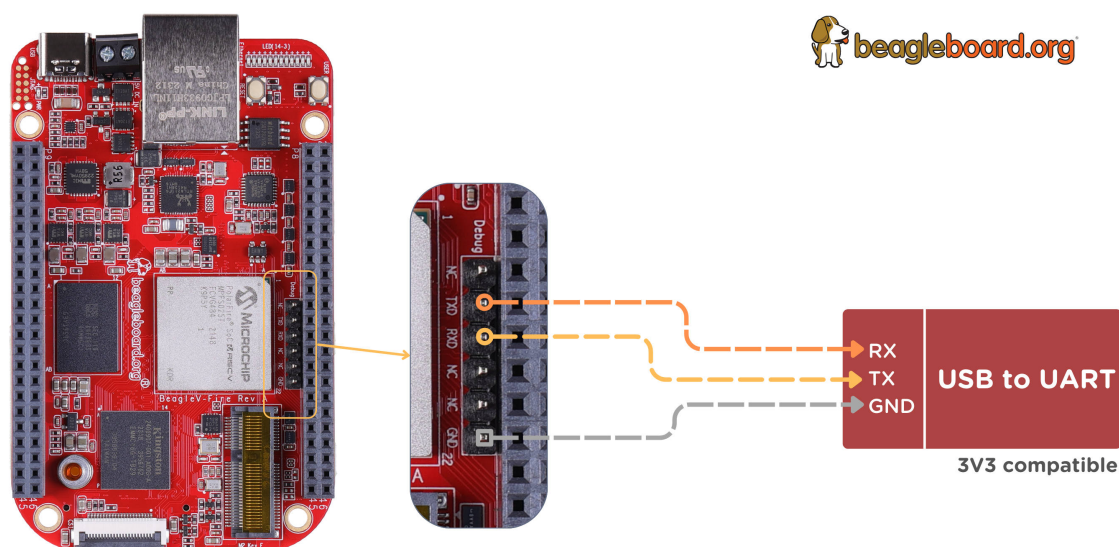
1. From drop-down select Program action

2. Click on RUN button
3. Shows the progress

If you see a lot of green color and progress bar says *PASSED* then well done you have successfully flashed the gateway image on your BeagleV-Fire board.

### 5.2.3 Flashing eMMC

Connect to BeagleV-Fire UART debug port using a 3.3v USB to UART bridge.



Now you can run `tio <port>` in a terminal window to access the UART debug port connection. Once you are connected properly you can press the Reset button which will show you a progress bar like in the

```
HSS: decompressing from eNVM to L2 Scratch ... Passed
DDR training ...
█ 60% [ ..... ]
```

Once you see that progress bar on your screen you can start pressing any button (0-9/a-z) which will stop the board from fully booting and you'll be able to access Hart Software Services (HSS) prompt. BeagleV-Fire's eMMC content is written by the Hart Software Services (HSS) using the `usbdmhc` command. The HSS `usbdmhc` command exposes the eMMC as a USB mass storage device USB type C connector.

Once you see `>>` you can execute the commands below:

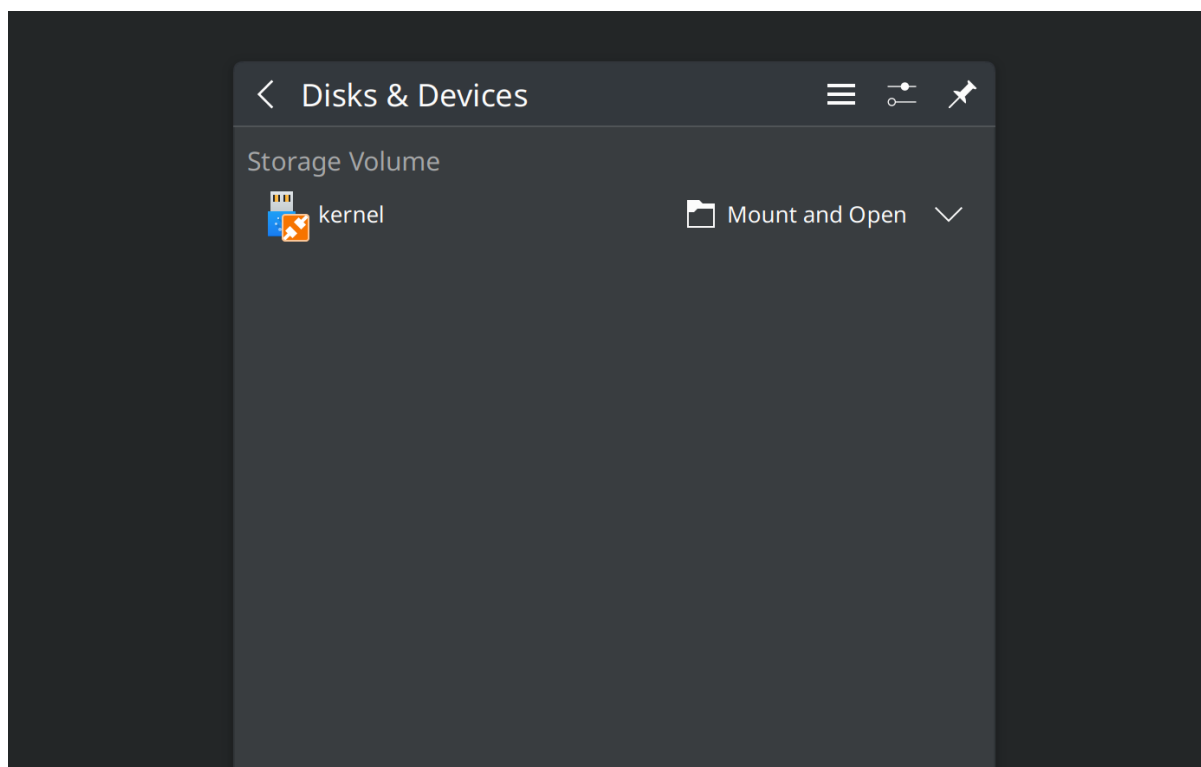
1. `>> mmc`
2. `>> usbdmhc`

After executing the commands above your BeagleV-Fire's eMMC will be exposed as a mass storage device like shown in the image below:

Once your board is exposed as a mass storage device you can use [Balena Etcher](#) to flash the `sdcad.img` on your BeagleV-Fire's eMMC.

Select image





1. Select the `sdcard.img` file from your local drive storage.
2. Click on select target.

Select Target

1. Select `MCC PolarFireSoC_msd` as target.
2. Click `Select (1)` to proceed.

Flash image

1. Click on `Flash!` to flash the `sdcard.img` on BeagleV-Fire eMMC storage.

Congratulations! with that done you have fully updated BeagleV-Fire board with up to date gateway image on it's PolarFire SoC's FPGA Fabric and linux image on it's eMMC storage.

## 5.3 Microchip FPGA Tools Installation Guide

Instructions for installing the Microchip FPGA tools on a Ubuntu 20.04 desktop.

---

**Important:** We will be providing instances of Libero that you can run from [git.beagleboard.org](https://git.beagleboard.org)'s gitlab-runners such that you do not need to install the tools on your local machine.

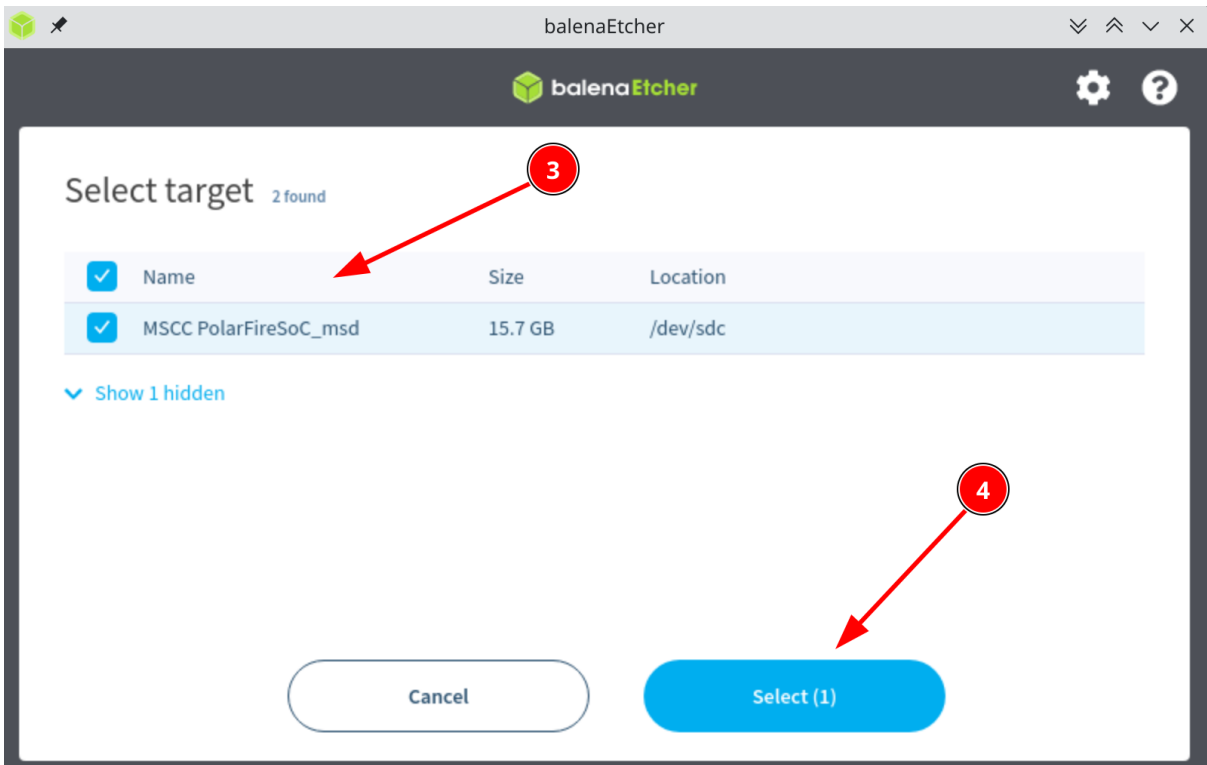
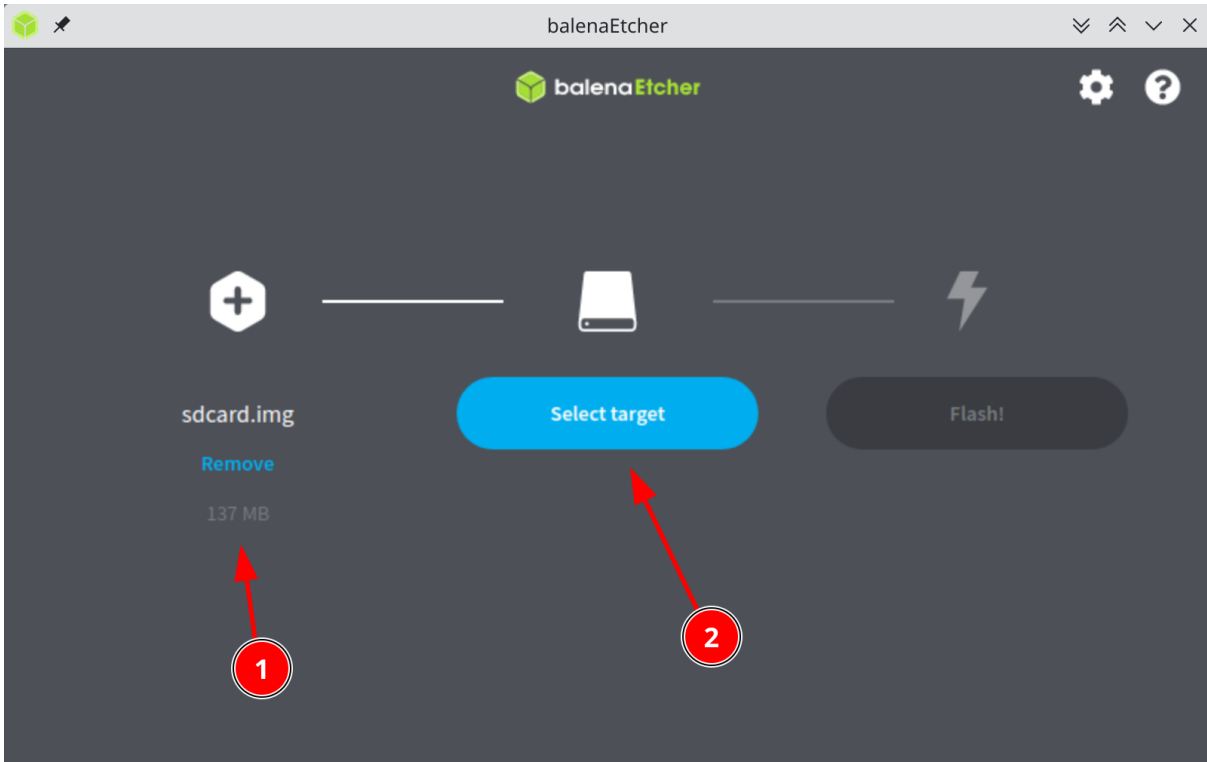
---

**Todo:** Make sure people know about the alternative and we provide links to details on that before we send them down this process.

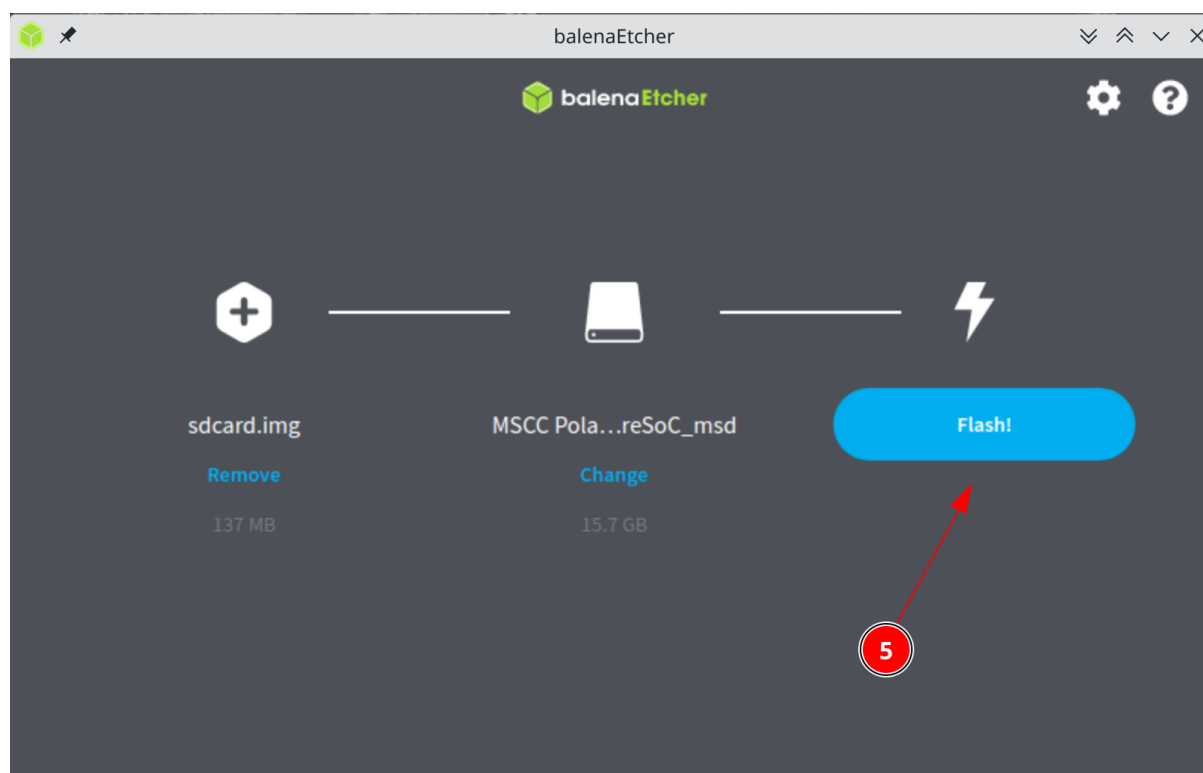
---

### 5.3.1 Install Libero 2022.3

- Download installer from the [Microchip's fpga and soc design tools section](#).







- Install Libero

```
unzip Libero_SoC_v2022.3_lin.zip
cd Libero_SoC_v2022.3_lin/
./launch_installer.sh
```

**Important:** Do not use the default location suggested by the Libero installer. Instead of `/usr/local/Microchip/Libero_SoC_v2022.3` install into `~/Microchip/Libero_SoC_v2022.3`

Run the post installation script which will install missing packages:

```
sudo /home/<USER-NAME>/Microchip/Libero_SoC_v2022.3/Logs/req_to_install.sh
```

No need to run the FlashPro hardware installation scripts. This will be taken care of as part of the SoftConsole installation.

### 5.3.2 Install SoftConsole 2022.2

- Download intaller from [Microchip website](#).

```
sudo chmod +x Microchip-SoftConsole-v2022.2-RISC-V-747-linux-x64-installer.
→run
./Microchip-SoftConsole-v2022.2-RISC-V-747-linux-x64-installer.run
```

Accept the license, Click Forward, Finish.

Perform the post installation steps as described in the html file opened when you click Finish.

---

**Important:** Please pay special attention to the “Enabling non-root user to access FlashPro” section of the post-installation instructions. This will actually allow you to program the board using Libero.

---

### 5.3.3 Install the Libero licensing daemon

Download the 64 bit Licensing Daemons from the [Microchip’s daemons section](#)

- [Linux\\_Licensing\\_Daemon\\_11.16.1\\_64-bit.tar.gz](#)
- [Windows\\_Licensing\\_Daemon\\_11.16.1\\_64-bit.zip](#)

Copy the downloaded file to the Microchip directory within your home directory and untar it.

```
cd ~/Microchip
tar -xvf Linux_Licensing_Daemon_11.16.1_64-bit.tar.gz
```

Install the Linux Standard Base:

```
sudo apt-get update
sudo apt-get -y install lsb
```

### 5.3.4 Request a Libero Silver license

- Visit [microchip’s fpga and soc design tool licensing page](#)
- Click on Register a free license button and Register or login.
- Click “Request Free License” and choose “Libero Silver 1Yr Floating License for Windows/Linux Server” from the list.
- Enter you MAC address and click register.

---

**Note:** A MAC address looks something like 12:34:56::78:ab:cd when you use the “ip address” command to find out its value on your Linux machine. However, you need to enter it as 123456abcd in this dialog box.

---

You will get an email with a license.dat file. Copy it into the ~/Microchip/license directory. Edit the License.dat file to replace the <put.hostname.here> string with... localhost.

### 5.3.5 Execute tool setup script

Download the script:

Listing 5.1: Libero environment and license setup script

```
#!/bin/bash

→#=====
# Edit the following section with the location where the following tools are
# installed:
#   - SoftConsole (SC_INSTALL_DIR)
#   - Libero (LIBERO_INSTALL_DIR)
#   - Licensing daemon for Libero (LICENSE_DAEMON_DIR)
```

(continues on next page)

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```

→#=====
export SC_INSTALL_DIR=/home/$USER/Microchip/SoftConsole-v2022.2-RISC-V-747
export LIBERO_INSTALL_DIR=/home/$USER/Microchip/Libero_SoC_v2023.2
export LICENSE_DAEMON_DIR=/home/$USER/Microchip/Linux_Licensing_Daemon
export LICENSE_FILE_DIR=/home/$USER/Microchip/license

→#=====
# The following was tested on Ubuntu 20.04 with:
# - Libero 2023.2
# - SoftConsole 2022.2

→#=====

#
# SoftConsole
#
export PATH=$PATH:$SC_INSTALL_DIR/riscv-unknown-elf-gcc/bin
export FPGENPROG=$LIBERO_INSTALL_DIR/Libero/bin64/fpgenprog

#
# Libero
#
export PATH=$PATH:$LIBERO_INSTALL_DIR/Libero/bin:$LIBERO_INSTALL_DIR/Libero/
→bin64
export PATH=$PATH:$LIBERO_INSTALL_DIR/Synplify/bin
export PATH=$PATH:$LIBERO_INSTALL_DIR/Model/modeltech/linuxacoem
export LOCALE=C
export LD_LIBRARY_PATH=/usr/lib/i386-linux-gnu:$LD_LIBRARY_PATH

#
# Libero License daemon
#
export LM_LICENSE_FILE=1702@localhost
export SNPSLMD_LICENSE_FILE=1702@localhost

$LICENSE_DAEMON_DIR/lmgrd -c $LICENSE_FILE_DIR/License.dat -l $LICENSE_FILE_
→DIR/license.log

```

```
setup-microchip-tools.sh
```

Source the script:

```
./setup-microchip-tools.sh
```

---

**Important:** Do not forget the leading dot. It matters. You will need to run this every time you restart your machine.

---

You can then start Libero to open an existing Libero project.

```
libero
```

However you will more than likely want to use Libero to run a TCL script that will build a design for you.

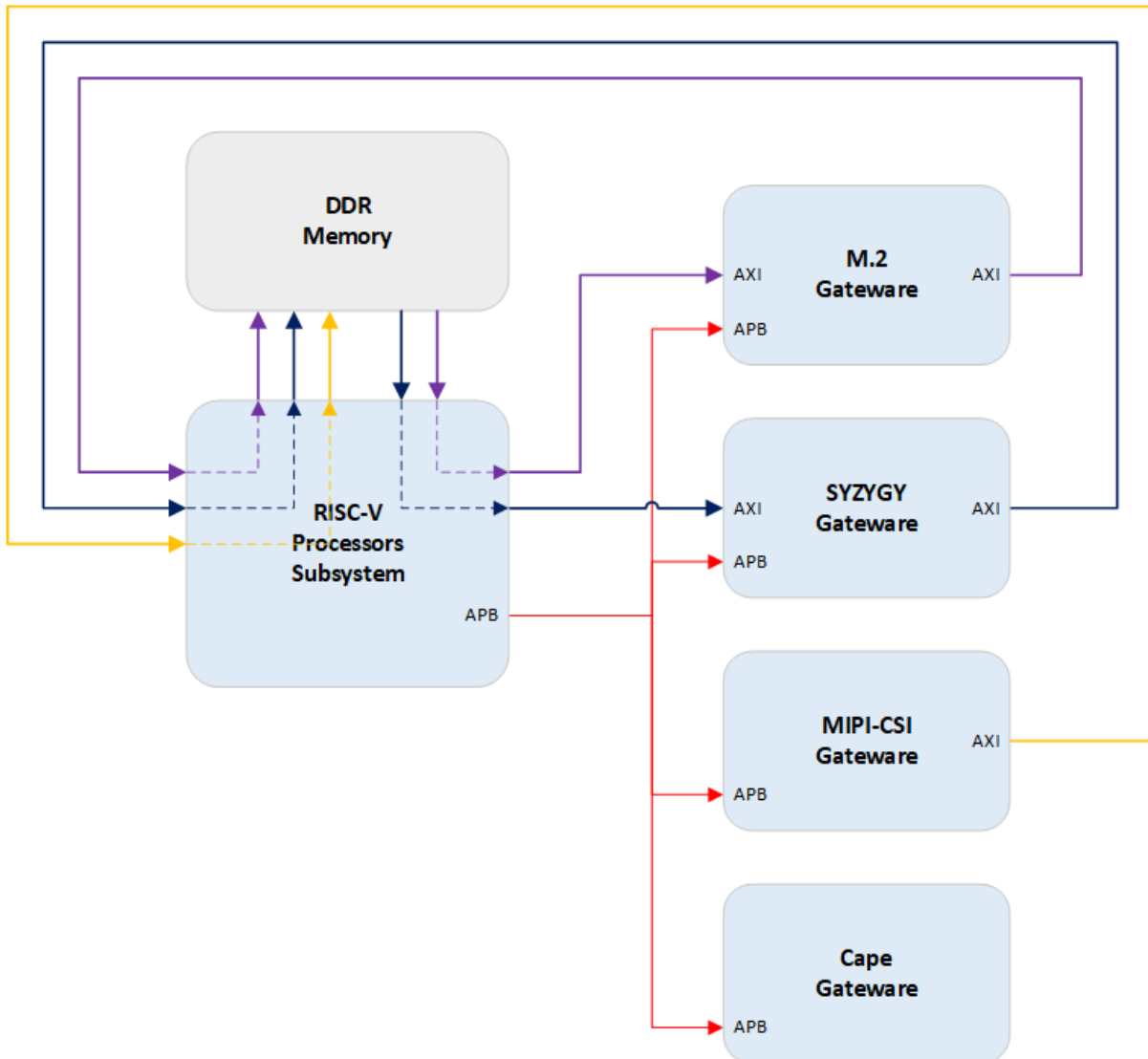
```
libero SCRIPT:BUILD_A_DESIGN.tcl
```

## 5.4 Gateware Design Introduction

The PolarFire SoC device used on BeagleV-Fire is an SoC FPGA which includes a RISC-V processors subsystem and a PolarFire FPGA on the same die. The gateware configures the Microprocessor subsystem's hardware and programs the FPGA with digital logic allowing customization of the use of BeagleV-Fire connectors.

### 5.4.1 Gateware Architecture

The diagram below is a simplified overview of the gateware's structure.



The overall gateware is made-up of several blocks, some of them interchangeable. These blocks are all clocked and reset by another "Clock and Resets" block not showed in the diagram for clarity.

Each gateway block is associated with one of BeagleV-Fire's connectors.

All gateway blocks have an AMBA APB target interface for software to access control and status registers defined by the gateway to operate digital logic defined by the gateway block. This is the software's control path into the gateway block.

Some gateway blocks also have an AMBA AXI target and/or source interfaces. The AXI interfaces are typically used to move high volume of data at high throughput in and out of DDR memory. For example, the M.2 gateway uses these interfaces to transfer data in and out of its PCIe root port.

## Cape Gateware

The cape gateway handles the P8 and P9 connectors signals. This is where support for specific capes is implemented.

This is a very good place to start learning about FPGA and how to customize gateway.

## SYZGY Gateway

**The SYZGY gateway handles the high-speed connector signals. This connector includes:**

- up to three transceivers capable of 12.7Gbps communications
- One SGMII interface
- 10 high-speed I/Os
- Clock inputs

There is a lot of fun that can be had with this interface given its high-speed capabilities.

Please note that only two transceivers can be used when the M.2 interface is enabled.

## MIPI-CSI Gateway

The MIPI gateway handles the signals coming from the camera interface.

Gateway for the MIPI-CSI interface is Work-In-Progress.

## M.2 Gateway

The M.2 gateway implements the PCIe interface used for Wi-Fi modules. It connects the processor subsystem to the PCIe controller associated with the transceivers bank.

There is limited fun to have here. You either include this block or not in your bitstream.

The M.2 gateway uses one of the four available 12.7 Gbps transceivers. Only two out of the three SYZGY transceivers can be used when the M.2 is included in the bitstream. This gateway needs to be omitted from the bitstream if you want to use all three 12.7Gbps transceivers on the SYZGY high-speed connector.

## RISC-V Processors subsystem

The RISC-V Processors Subsystem also includes some gateway mostly dealing with exposing AMBA bus interfaces for the other gateway blocks to attach to. It also handles immutable aspects of the gateway related to how some PolarFire-SoC signals are used to connect BeagleV-Fire peripherals such as the ADC and EEPROM. As such the RISC-V Processors Subsystem gateway is not intended to be customized.

## 5.5 How to retrieve BeagleV-Fire's gateway version

There are two methods to find out what gateway is programmed on a board.

### 5.5.1 Device Tree

The device tree overlays contains the list of gateway blocks included in the overall gateway design. You can retrieve that information using the following command:

```
tree /proc/device-tree/chosen/overlays/
```

This should give an output similar to the one below.

```
beagle@BeagleV:~$ tree /proc/device-tree/chosen/overlays/
/proc/device-tree/chosen/overlays/
├── name
├── PCIE-M2-GATEWARE
└── ROBOTICS-CAPE-GATEWARE

1 directory, 3 files
```

The gateway version can be retrieve by reading one of the overlay files. For example, the command:

```
cat /proc/device-tree/chosen/overlays/ROBOTICS-CAPE-GATEWARE
```

should result in:

```
beagle@BeagleV:~$ cat /proc/device-tree/chosen/overlays/ROBOTICS-CAPE-GATEWARE
BVF-0.3.0-5-g3e0d3380beagle@BeagleV:~$
```

where the result of a “git describe” command on the gateway repository is displayed. This provides the most recent tag on the gateway repository followed by information about additional commits if some exist. In the example above, the gateway was created from a gateway repository hash 3e0d338 which is 5 commits more recent than tag BVF-0.3.0.

### 5.5.2 Bootloader messages

The Hart Software Services display the gateway design name and design version retrieve from the FPGA at system start-up.

```
[5.528316] Design Info:
        Design Name: DEV_ROBOTICS_3E0D338F3C2574145
        Design Version: 02.00.1
```

The design name is the name of the build option selected when using the bitstream-builder to generate the bitstream. The number at the end of the design name is the hash of the gateway repository used to build the bitstream.

The design version is specified as part of the bitstream-builder build configuration option.

Please note that design name “BVF\_GATEWARE” indicates that the bitstream used to program the board was generated directly from the gateway repositories scripts and not the bitstream-builder. You might see this when customizing the gateway. Seeing “BVF\_GATEWARE” as the design name should be a warning sign that there is a disconnect between the hardware and software on your board.

## 5.6 Gateway Full Build Flow

### 5.6.1 Introduction

BeagleV-Fire gateway is made up of several components:

- Digital design for the FPGA fabric.

- Microprocessor Subsystem (MSS) configuration containing MSS configuration register values.
- A zero stage bootloader (HSS).
- A set of device tree overlays describing the content of the FPGA fabric.

The FPGA's digital design is a combination of:

- HDL/Verilog source code
- TCL scripts configuring IP blocks
- TCL scripts stitching IP blocks together
- Microprocessor Subsystem (MSS) configuration describing the MSS port list
- Pin, placement and timing constraints

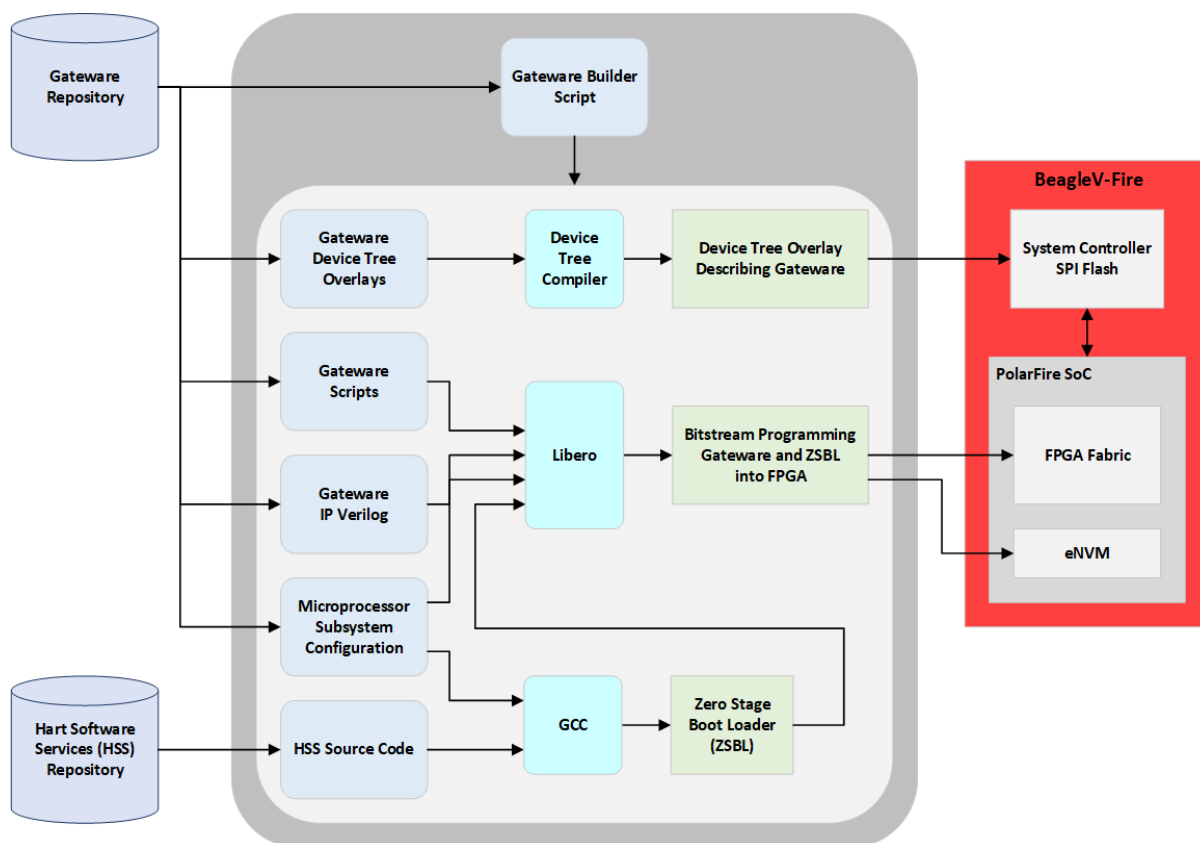
The Hart Software Service (HSS) zero stage bootloader

- Configures the PolarFire SoC chip.
- Retrieves the next boot stage from eMMC and hand-over to the next boot stage (e.g. u-boot)
- Makes the board appear as a USB mass-storage for populating the eMMC with secondary boot-loader and operating system image.

The chip configuration applied by the HSS includes the configuration of:

- Clocks
- Memory controllers
- IOs
- Transceivers

Of course all these components need to be in synch with each other for the system to work properly. This is the reason for using a gateway build system rather than building and tracking each component individually.



### 5.6.2 Programming artifacts

The gateway builder for BeagleV-Fire produces two programming artifacts:

- A bitstream containing the FPGA fabric and eNVM programming
- A device tree overlay describing the FPGA content.

These two artifacts are packaged differently depending on the programming method. They are merged into a single programming file for DirectC (.dat) and FlashPro Express (.job). They are kept separate for Linux programming (mpfs\_bitstream.spi and mpfs\_dtbo.spi).

### 5.6.3 Programming BeagleV-Fire with new gateway

There are several methods possible for programming the BeagleV-Fire with new gateway:

- Linux script executed on the BeagleV-Fire board.
- Running DirectC on another single board computer
- Using Microchip's FlashPro Express

#### Linux script

This is the recommended approach. It does not require any additional hardware. Simply run the script located in `/usr/share/beagleboard/gateway`. You should use this method unless you have soft-bricked your BeagleV-Fire.

#### DirectC

This approach uses a single board computer (SBC) connected to the BeagleV-Fire JTAG port. The SBC bit-bangs the FPGA programming protocol over GPIOs. This approach is only required for recovering a soft-bricked BeagleV-Fire.

#### FlashPro Express

This approach uses Microchip's FlashPro Express programming software and a FlashPro6 JTAG programmer. I would recommend using the Linux script even if you are an existing Microchip FPGA user with all the tools. This approach makes most sense when doing bare metal software development and already have a FlashPro programmer and don't care about device tree overlays.

## 5.7 Gateway TCL Scripts Structure

This document describes the structure of the gateway TCL scripts. It is of interest to understand how to extend or customize the gateway.

The [Liberio SoC TCL Command Reference Guide](#) describes the TCL command used in the gateway scripts.

### 5.7.1 Gateway Project

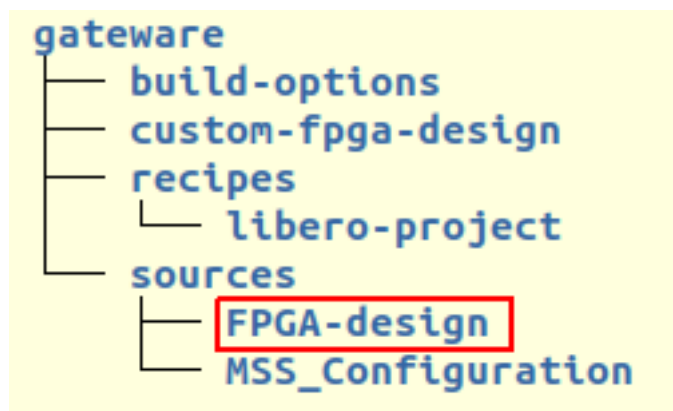
The gateway project is made up of:

- TCL scripts
- HDL/Verilog source code
- IO pin constraints



- Placement constraints
- Device tree overlays

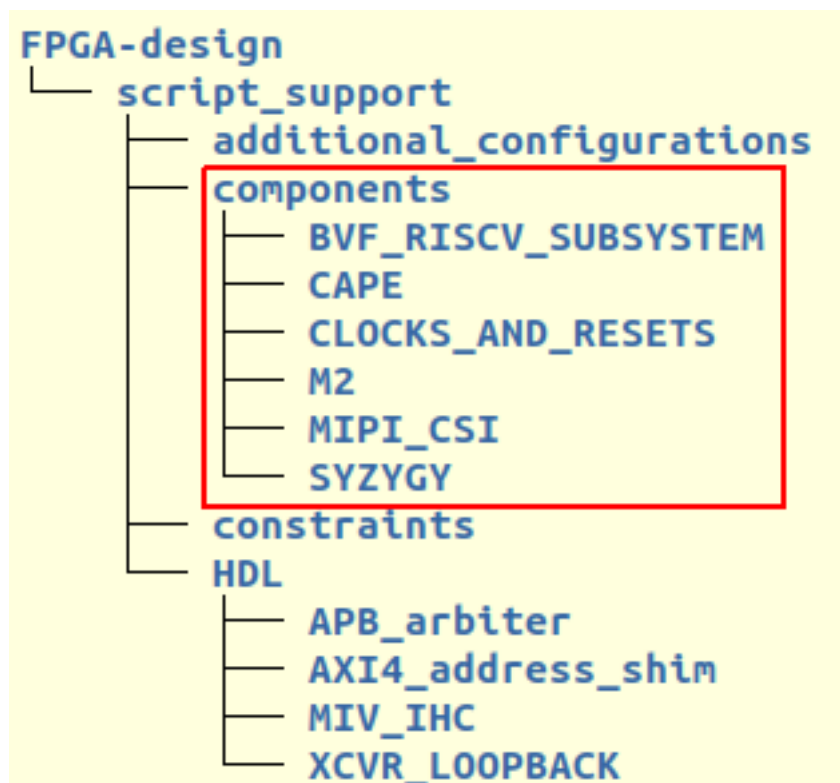
All these files are found in the FPGA-design directory.



### 5.7.2 Gateware Components

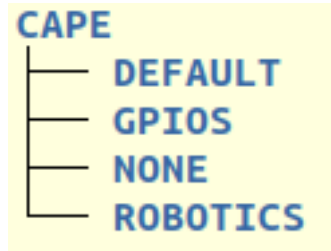
The gateware is organized into 6 components:

- Clocks and reset control
- A base RISC-V microprocessor subsystem
- Cape interface
- M.2 interface
- MIPI camera interface
- SYZYGY high speed interface



### 5.7.3 Gateware Build Options

Each interface component may have a number of build options. For example, which cape will be supported by the generated gateware.



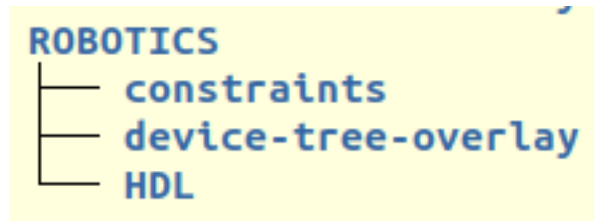
The name of the directories within the component's directory are the option names passed to the top Libero BUILD\_BVF\_GATEWATE.tcl script. These directory names are the option name specified in the bitstream builder's build option YAML files.

The gateware is extended or customized by creating additional directories within the component directory of interest. For example, add a MY\_CUSTOM\_CAPE directory under the CAPE directory to add a gateware build option to support a custom cape.

### 5.7.4 Gateware Component Directories

The component directory contains subdirectories for:

- Constraint files
- Device tree overlay
- Optional HDL/Verilog source code



#### Gateware TCL Scripts

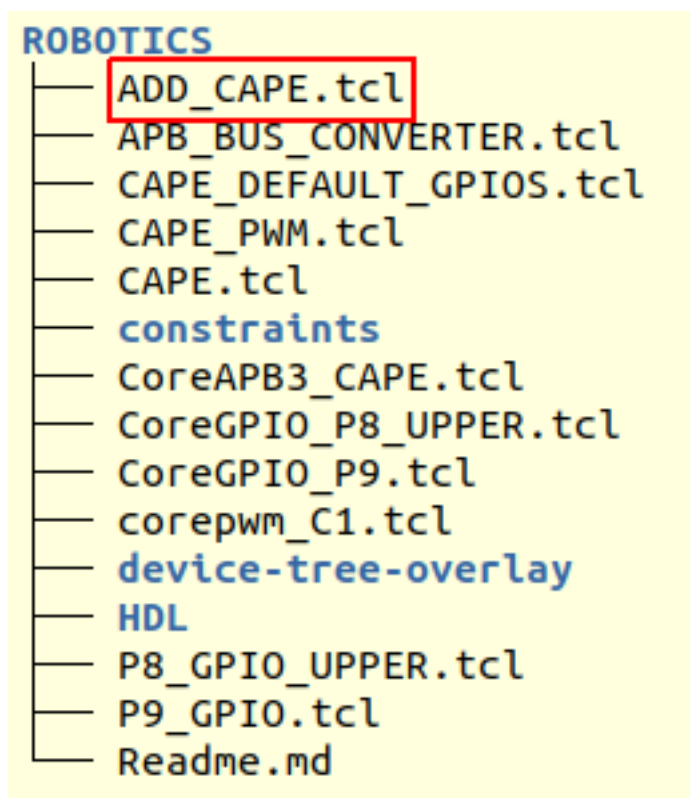
The component directory contains the TCL scripts executed by Libero to generate the gateware. The TCL script framework executes a hand-crafted ADD\_<COMPONENT\_NAME>.tcl script which instantiates the component and stitches it to the base RISC-V subsystem and top level IOs. The other TCL scripts are typically IP configuration scripts and SmartDesign stitching scripts.

## 5.8 Customize BeagleV-Fire Cape Gateware Using Verilog

This document describes how to customize gateware attached to BeagleV-Fire's cape interface using Verilog as primary language. The methodology described can also be applied when using other HDL languages.

It will describe:

- How to generate programming bitstreams without requiring the installation of the Libero FPGA toolchain on your development machine.
- How to use the cape Verilog template



- How to use the git.beagleboard.org CI infrastructure to generate programming bitstreams for your custom gateway

Steps:

1. Fork BeagleV-Fire gateway repository on git.beagleboard.org
2. Create a custom gateway build option
3. Rename a copy of the cape gateway Verilog template
4. Customize the cape's Verilog source code
5. Commit and push changes to your forked repository
6. Retrieve the forked repositories artifacts
7. Program BeagleV-Fire with your custom bitstream

### 5.8.1 Fork BeagleV-Fire Gateway Repository

---

**Important:** All new users need to be manually approved to protect from BOT spam. You will not be able to fork the Gateway Repository until you have been approved. A request to 'the forum <<https://forum.beagleboard.org/t/requesting-access-to-gitlab-to-fork-gateway/37494>>' may expedite the process.

---

Navigate to BeagleV-Fire's [gateway source code repository](#).

Click on the `Forks` button on the top-right corner.

On the Fork Project page, select your namespace and adjust the project name to help you manage multiple custom gateway (e.g. `my-lovely-gateway`). Click the `Fork project` button.



Fig. 5.1: BeagleV-Fire gateway repo fork button

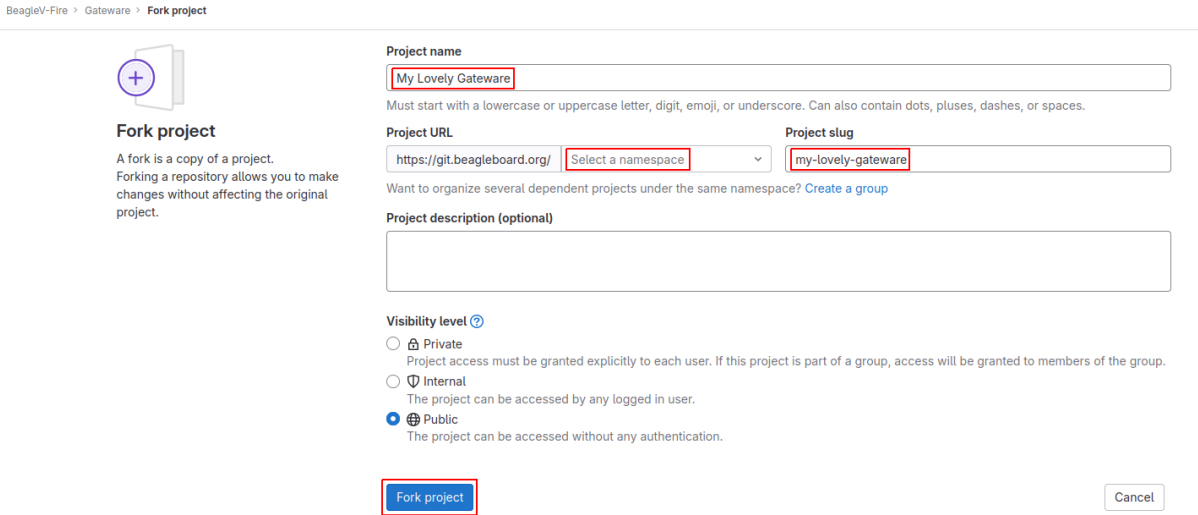


Fig. 5.2: Create gateway fork

### Clone the forked repository

```
git clone git@git.beagleboard.org:<MY-NAMESPACE>/my-lovely-gateway.git
```

Where <MY-NAMESPACE> is your Gitlab username or namespace.

### 5.8.2 Create A Custom Gateway Build Option

BeagleV-Fire's gateway build system uses "build configuration" YAML files to describe the combination of gateway components options that will be used to build the gateway programming bitstream. You need to create one such file to describe to the gateway build system that you want your own custom gateway to be built. You need to have one such file describing your gateway in directory `custom-fpga-design`.

Let's modify the `./custom-fpga-design/my_custom_fpga_design.yaml` build configuration file to specify that your custom cape gateway should be included in the gateway bitstream. In this instance will call our custom cape gateway `MY_LOVELY_CAPE`.

```
HSS:
  type: git
  link: https://git.beagleboard.org/beaglev-fire/hart-software-services.git
  branch: develop-beaglev-fire
  board: bvf
gateway:
  type: sources
  build-args: "M2_OPTION:NONE CAPE_OPTION:MY_LOVELY_CAPE" # ?
  unique-design-version: 9.0.2
```

① On the gateway build-args line, replace `VERILOG_TUTORIAL` with `MY_LOVELY_CAPE`.

**Note:** The `custom-fpga-design` directory has a special meaning for the Beagleboard Gitlab CI system. Any build configuration found in this directory will be built by the CI system. This allows generating FPGA

programming bitstreams without the requirement for having the Microchip FPGA toolchain installed on your computer.

---

### 5.8.3 Rename A Copy Of The Cape Gateway Verilog Template

#### Move to the cape gateway source code

```
cd my-lovely-gateway/sources/FPGA-design/script_support/components/CAPE
```

#### Create a directory that will contain your custom cape gateway source code

```
mkdir MY_LOVELY_CAPE
```

#### Copy the cape Verilog template

```
cp -r VERILOG_TEMPLATE/* ./MY_LOVELY_CAPE/
```

### 5.8.4 Customize The Cape's Verilog Source Code

#### Move to your custom gateway source directory

```
cd MY_LOVELY_CAPE
```

You will need to first edit the `ADD_CAPE.tcl` TCL script to use your source code within your custom gateway directory and not the Verilog template source code. In this example this means using source code within the `MY_LOVELY_CAPE` directory rather the `VERILOG_TEMPLATE` directory.

#### Edit `ADD_CAPE.tcl`

Replace `VERILOG_TEMPLATE` with `MY_LOVELY_CAPE` in file `ADD_CAPE.tcl`.

```
#-----  
↪---  
# Import HDL source files  
#-----  
↪---  
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/  
↪apb_ctrl_status.v}  
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/  
↪P8_IOPADS.v}  
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/  
↪P9_11_18_IOPADS.v}  
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/  
↪P9_21_31_IOPADS.v}  
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/  
↪P9_41_42_IOPADS.v}  
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/  
↪CAPE.v}
```

Add the path to your additional Verilog source code files.

```

#-----
# Import HDL source files
#-----
#-----
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/
↳blinky.v} // ①
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/
↳apb_ctrl_status.v}
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/
↳P8_IOPADS.v}
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/
↳P9_11_18_IOPADS.v}
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/
↳P9_21_31_IOPADS.v}
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/
↳P9_41_42_IOPADS.v}
import_files -hdl_source {script_support/components/CAPE/MY_LOVELY_CAPE/HDL/
↳CAPE.v}

```

① In our case we will be adding a new Verilog source file called `blinky.v`.

You will only need to revisit the content of `ADD_CAPE.tcl` if you want to add more Verilog source files or want to modify how the cape interfaces with the rest of the gateway (RISC-V processor subsystem, clock and reset blocks).

### Customize The Cape's Verilog source code

We will add a simple Verilog source file, `blinky.v`, in the `MY_LOVELY_CAPE` directory. Code below:

```

`timescale 1ns/100ps
module blinky(
input    clk,
input    resetn,
output   blink
);

reg [22:0] counter;

assign blink = counter[22];

always@(posedge clk or negedge resetn)
begin
    if(~resetn)
        begin
            counter <= 16'h0000;
        end
    else
        begin
            counter <= counter + 1;
        end
end
endmodule

```

Let's connect the `blinky` Verilog module within the cape by editing the `CAPE.v` file.

Add the instantiation of the `blinky` module:

```

//-----P9_41_42_IOPADS
P9_41_42_IOPADS P9_41_42_IOPADS_0 (

```

(continues on next page)

(continued from previous page)

```

// Inputs
.GPIO_OE  ( GPIO_OE_const_net_3 ),
.GPIO_OUT ( GPIO_OUT_const_net_3 ),
// Outputs
.GPIO_IN  (   ),
// Inouts
.P9_41    ( P9_41 ),
.P9_42    ( P9_42 )
);

//-----blinky
blinky blinky_0(           // ?
    .clk      ( PCLK ),      // ?
    .resetn   ( PRESETN ),  // ?
    .blink    ( BLINK )     // ?
);

endmodule

```

- ① Create a blinky module instance called blinky\_0.
- ② Connect the clock using the existing PCLK wire.
- ③ Connect the reset using the existing PRESETS wire.
- ④ Connect the blinky's blink output using the BLINK wire. This BLINK wire needs to be declared.

Add the BLINK wire:

```

wire      PCLK;
wire      PRESETN;
wire      BLINK;           // ?
wire [31:0] APB_SLAVE_PRDATA_net_0;
wire [27:0] GPIO_IN_net_1;

```

- ① Create a wire called BLINK.

The BLINK wire will be used to connect the blinky module's output to a top level output connected to an LED. Do you see where this is going?

Now for the complicated part. We are going to change the wiring of the bi-directional buffers controlling the cape I/Os including the user LEDs.

The original code populates two 43 bits wide wires for controlling the output-enable and output values of the P8 cape connector I/Os. The bottom 28 bits being controlled by the microprocessor subsystem's GPIO block.

```

//-----
↪-
// Concatenation assignments
//-----
↪-
assign GPIO_OE_net_0 = { 16'h0000 , GPIO_OE };
assign GPIO_OUT_net_0 = { 16'h0000 , GPIO_OUT };

```

We are going to hijack the 6th I/O with our blinky's output:

```

//-----
// Concatenation assignments
//-----
assign GPIO_OE_net_0 = { 16'h0000, GPIO_OE[27:6], 1'b1, GPIO_OE[4:0] };  ↪
↪ // ?
assign GPIO_OUT_net_0 = { 16'h0000 , GPIO_OUT[27:6], BLINK, GPIO_OUT[4:0] }; ↪
↪ // ?


```

- ① Tie high the output-enable of the 6th bit to constantly enable that output.
- ② Control the 6th output from the blink module through the WIRE wire.

### Edit The Cape's Device Tree Overlay

You should always have a device tree overlay associated with your gateway even if there is limited control from Linux. The device tree overlay is very useful to identify which gateway is currently programmed on your BeagleV-Fire.

```
/dts-v1/;
/plugin/;

&{/chosen} {
    overlays {
        MY-LOVELY-CAPE-GATEWARE = "GATEWARE_GIT_VERSION"; // 
    };
};
```

- ① Replace VERILOG-CAPE-GATEWARE with MY-LOVELY-CAPE-GATEWARE.

This change will result in MY-LOVELY-CAPE-GATEWARE being visible in `/proc/device-tree/chosen/overlays` at run-time, allowing to check that my lovely gateway is successfully programmed on BeagleV-Fire.

### 5.8.5 Commit And Push Changes To Your Forked Repository

Move back up to the root directory of your gateway project. This is the my-lovely-gateway directory in our current example.

Add the my-lovely-gateway/sources/FPGA-design/script\_support/components/CAPE/MY\_LOVELY\_CAPE directory content to your git repository.

```
git add sources/FPGA-design/script_support/components/CAPE/MY_LOVELY_CAPE/
```

Commit changes to my-lovely-gateway/custom-fpga-design/my\_custom\_fpga\_design.yaml

```
git commit -m "Add my lovely gateway."
```

Push changes to your beagleboard Gitlab repository:

```
git push
```

### 5.8.6 Retrieve The Forked Repositories Artifacts

Navigate to your forked repository. Click Pipelines in the left pane then the Download Artifacts button on the right handside. Select build-job:archive. This will result in an artifacts.zip file being downloaded.

### 5.8.7 Program BeagleV-Fire With Your Custom Bitstream

Unzip the downloaded artifacts.zip file. Go to the gateway-builds-tester/artifacts/bitstreams directory:

```
cd gateway-builds-tester/artifacts/bitstreams
```



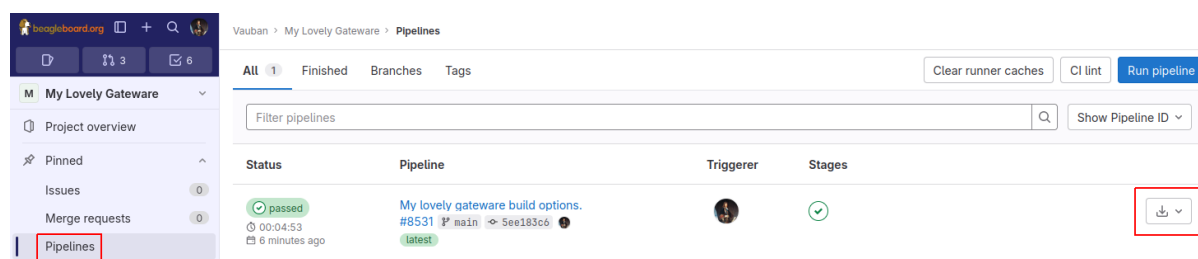


Fig. 5.3: gateway pipeline

On your Linux host development computer, use the scp command to copy the bitstream to BeagleV-Fire home directory, replacing <IP\_ADDRESS> with the IP address of your BeagleV-Fire.

```
scp -r ./my_custom_fpga_design beagle@<IP_ADDRESS>:/home/beagle/
```

On BeagleV-Fire, initiate the reprogramming of the FPGA with your gateway bitstream:

```
sudo /usr/share/beagleboard/gateway/changes-gateway.sh ./my_custom_fpga_
↪design
```

Wait for a couple of minutes for the BeagleV-Fire to reprogram itself.

You will see the 6th user LED flash once the board is reprogrammed. That's the Verilog you added blinking the LED.

On BeagleV-Fire, You can check that your gateway was loaded using the following command to see the device tree overlays:

```
tree /proc/device-tree/chosen/overlays/
```

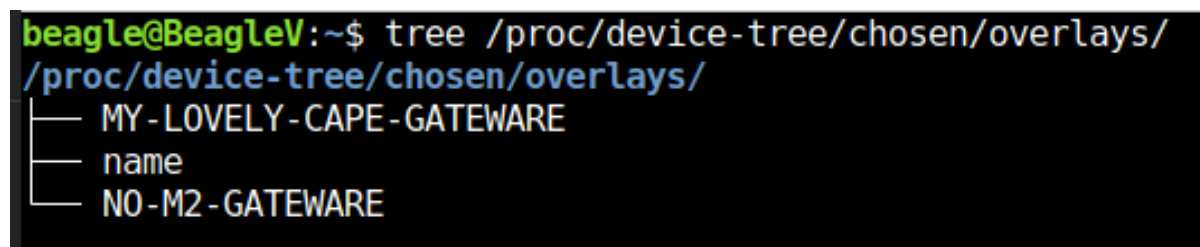


Fig. 5.4: gateway lovely overlay

## Chapter 6

# Support

All support for BeagleV Fire design is through BeagleBoard.org community at [BeagleBoard.org forum](https://beagleboard.org/forum).

### 6.1 Production board boot media

---

**Todo:** Add production boot media link in `_static/epilog/production.image` and reference it here.

---

### 6.2 Certifications and export control

#### 6.2.1 Export designations

---

**Todo:** update details

---

- HS: 8471504090
- US HS: 8543708800
- EU HS: 8471707000

#### 6.2.2 Size and weight

---

**Todo:** update details

---

- Bare board dimensions: 86.38\*54.61\*18.8mm
- Bare board weight: 45.8g
- Full package dimensions: 140 x 100 x 40 mm
- Full package weight: 106g

## 6.3 Additional documentation

### 6.3.1 Hardware docs

For any hardware document like schematic diagram PDF, EDA files, issue tracker, and more you can checkout the [BeagleV-Fire design repository](#).

### 6.3.2 Software docs

For BeagleV-Fire specific software projects you can checkout all the [BeagleV-Fire project repositories group](#).

### 6.3.3 Support forum

For any additional support you can submit your queries on our forum, <https://forum.beagleboard.org/tags/c/beaglev/15/fire>

### 6.3.4 Pictures

## 6.4 Change History

---

**Note:** This section describes the change history of this document and board. Document changes are not always a result of a board change. A board change will always result in a document change.

---

### 6.4.1 Board Changes

For all changes, see <https://git.beagleboard.org/beaglev-fire/beaglev-fire/>. Versions released into production are noted below.

Table 6.1: BeagleV-Fire board change history

Rev	Changes	Date	By
A	Initial production version	2023-11-02	JK