



BeagleBadge

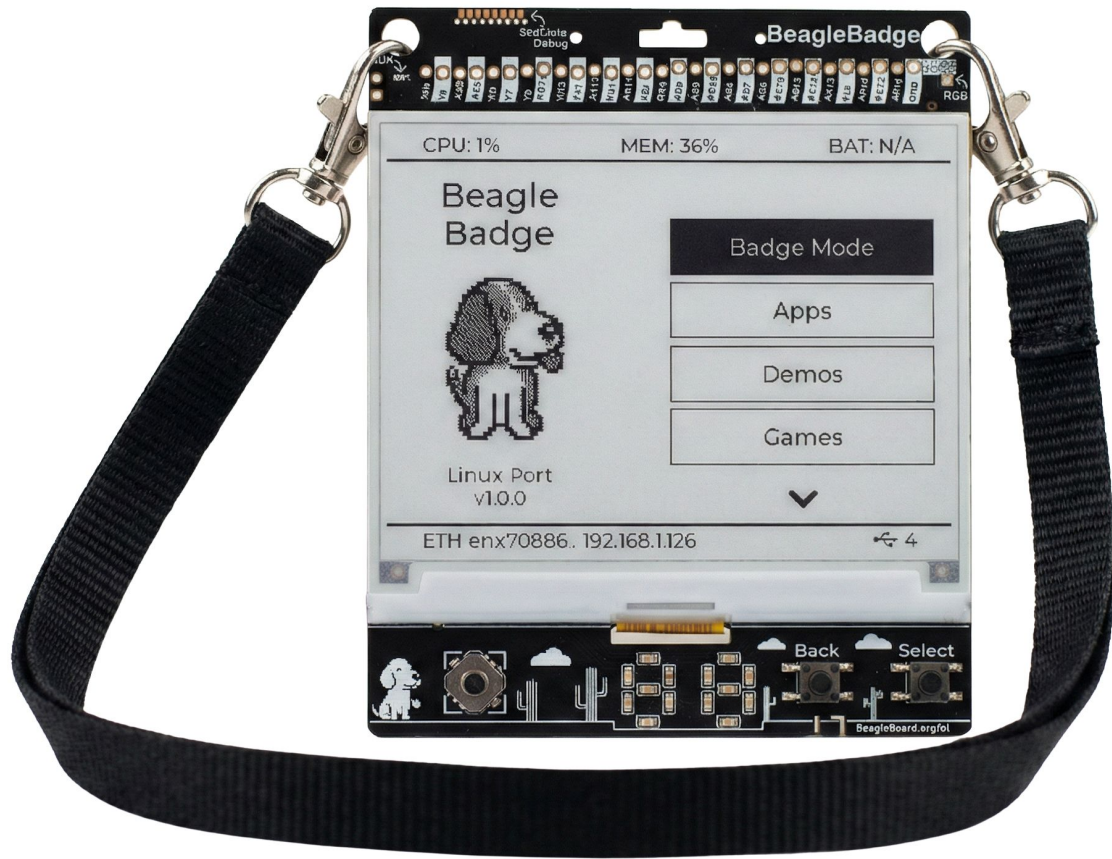


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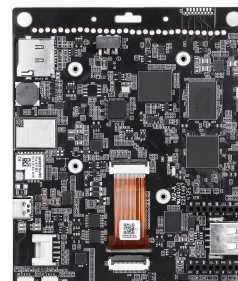
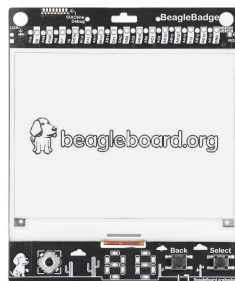
BeagleBadge is an open hardware, battery-powered Linux computer in a badge form factor. It pairs a 4.2 inch black-and-white ePaper display with a 5-way (4-directional and center) joystick, buttons, an RGB LED and two 7-segment digits. BeagleBadge also features 2.4GHz Wi-Fi 6, Bluetooth Low Energy and LoRa connectivity. On-board sensing includes a 6-axis accelerometer & gyroscope for position & orientation, plus an ambient light sensor. Two QWIC connectors, a Grove connector and a mikroBUS socket let you add off-the-shelf modules such as pulse oximeters, UV spectroscopy sensors, fingerprint readers, GPS receivers, haptic drivers, and audio boards. Use it to build interactive badges, wearable projects, health and environmental monitors, and human-machine interfaces.



Chapter 1

Introduction

BeagleBadge brings a new vision to wearable computing with e-ink display by combining built-in sensing with broad expansion flexibility. Built around the low-power Texas Instruments AM62L32 SoC and a 4.2 inch ePaper display. BeagleBadge pairs Wi-Fi 6, Bluetooth Low Energy 5.4, and LoRaWAN wireless connectivity. It has on-board 4-way joystick, tactile buttons, an RGB LED, and dual 7-segment displays for a complete human-machine interface out of the box. An onboard ambient light sensor, an IMU for precise position & orientation feedback, and temperature & humidity monitoring let you design intuitive, context-aware interactions. Beyond its core features, two QWIC connectors along with Grove and mikroBUS headers unlock thousands of additional sensors, actuators, pulse oximeters, UV spectroscopy, fingerprint readers, GPS, haptics, and audio applications. That modularity makes BeagleBadge a versatile innovation platform that enables rapid prototyping, research, and real-world solutions in health, environment, and human-machine interfaces, while remaining practical, scalable, and accessible to all.



1.1 BeagleBadge Features and Specifications

This section provides an overview of the key features and specifications of the BeagleBadge board, highlighting its built-in sensors and expansion capabilities. The table below summarizes the main features and their descriptions, showcasing the versatility and potential applications of the BeagleBadge platform.

Table 1.1: BeagleBadge Features and Specifications

Category	Item	Specification
Processor and memory	SoC	Texas Instruments AM62L32 , low-power SoC with display for IoT, HMI and general-purpose applications
	CPU	Dual-core Arm® Cortex®-A53 processor @ 1.25GHz
	RAM	256MB LPDDR4 (2Gb, 128M x 16bit) 1600MHz 3200Mbps
	Flash/non-volatile	256Mb OSPI flash
		32Kb EEPROM

continues on next page

Table 1.1 – continued from previous page

Category	Item	Specification
Networking	Wi-Fi & Bluetooth	802.11ax Wi-Fi 6 (2.4GHz) and Bluetooth Low Energy (BLE) 5.4 via BeagleBoard.org BeagleMod BM3301-1216 (TI CC3301), IPEX Gen 4 (MHF4) connector
Built-in sensors	LoRaWAN	Wio SX1262 module (u.FL connector)
	Sensors	1x IMU sensor 1x Ambient light sensor 1x Temperature & humidity sensor (not populated)
User interface	Input	1x Reset button 1x 4-way joystick button with press 2x Tactile buttons (Back and Select)
	Output	1x Passive buzzer 1x RGB status LED 2x 7-segment LED displays
Battery interface	Battery	Battery management with fuel gauge monitoring 1x BAT connector for BL-5C
Expansion/connectors	Display	Support 4.2 inch ePaper via 24-pin FPC connector MIPI DSI connector for LCD displays
	Power & debug	USB Type-C for power input and debug
	Ecosystem	1x mikroBUS connector 2x QWIIC connector 1x Grove connector
	Host & storage	1x USB 2.0 Type-A host 1x Micro-SD socket
Software	Base ports	Linux and Zephyr base ports with mainline roadmap
	Libraries	LVGL and MicroPython libraries for interactive ePaper display
	Examples	App store for programming examples
	Messaging	Meshtastic and ActivityPub integration for seamless off-grid messaging

1.2 Board Component Locations

The figures below locate each key component on the front and back of the board, with a table naming what each one does.

Todo

Replace both photographs with v1.0 board images. The current ones predate the Power button (S2 on [schematic sheet 20](#)). Label the Power button and the two [GPIO expansion headers](#) in the new annotations.

Front components location

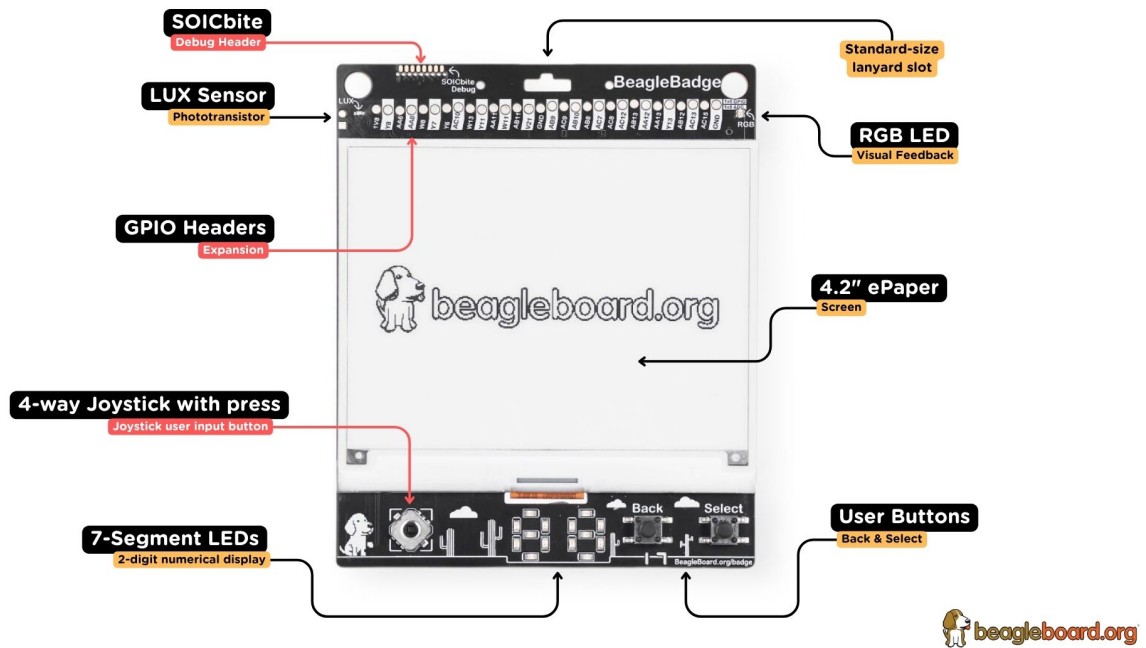


Fig. 1.1: BeagleBadge board front components location

Feature	Description
4.2" ePaper	400 x 300 black-and-white ePaper screen, the primary display
LUX sensor	Ambient light phototransistor
RGB LED	User controllable RGB LED for visual feedback
7-segment LEDs	2-digit numerical display
4-way joystick	Joystick user input button with centre press
User buttons	Back and Select tactile buttons
GPIO headers	1.8V GPIO and ADC expansion header along the top edge
SOICbite	Debug header, accessed with a standard SOIC test clip
Lanyard slot	Standard-size lanyard slot

Back components location

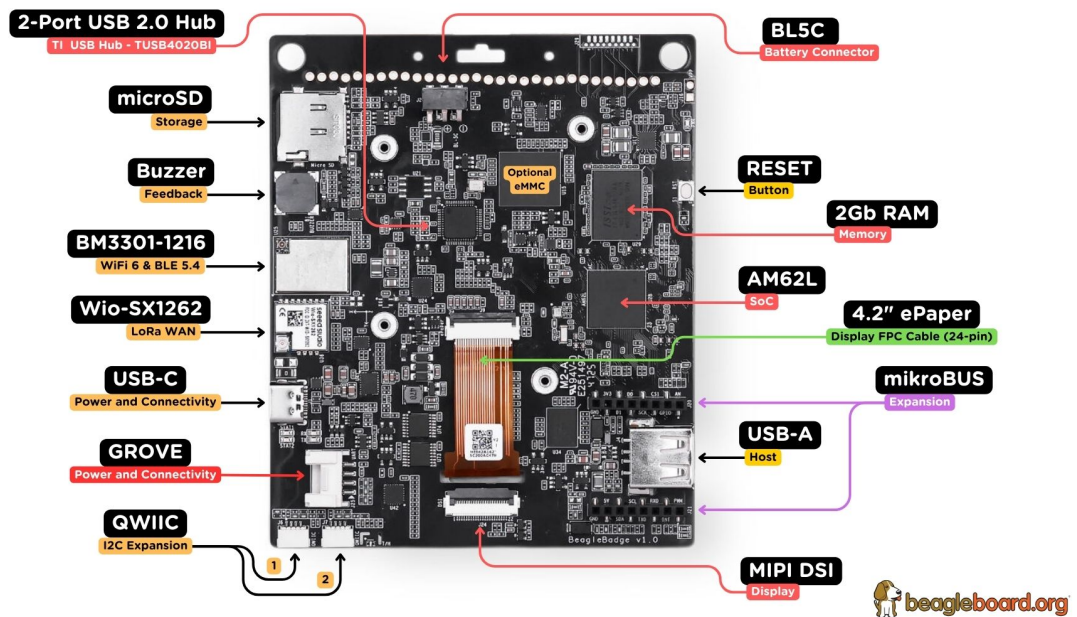


Fig. 1.2: BeagleBadge board back components location

Feature	Description
AM62L	Texas Instruments AM62L32 SoC, dual Arm Cortex-A53 at 1.25GHz
256MB RAM	LPDDR4 at 1600MHz, a 2Gb (128M x 16) device
Optional eMMC	eMMC footprint, not populated on v1.0. See eMMC footprint
BM3301-1216	BeagleMod module providing Wi-Fi 6 and BLE 5.4
Wio-SX1262	LoRaWAN module
2-port USB 2.0 hub	Texas Instruments TUSB4020BI
microSD	microSD card socket for storage
USB-C	Power and connectivity, also carries the serial debug console
USB-A	USB 2.0 Type-A host port for peripherals
mikroBUS	mikroBUS expansion socket for MikroElektronika Click boards
QWIIC	Two I2C expansion connectors, marked 1 and 2
Grove	Grove expansion connector
MIPI DSI	FPC connector for an LCD display
4.2" ePaper FPC	24-pin FPC connector for the ePaper display cable
BL5C	Battery connector for a BL-5C cell
RESET	Reset button
Buzzer	Passive buzzer for audible feedback

Chapter 2

Quick Start Guide

This chapter takes you from an unpacked board to a running console. Unlike most Beagles, BeagleBadge is built to run untethered from a single-cell lithium battery, so you can bring it up from USB Type-C, from a battery, or from both at once while the battery charges.

Every connector and control named here is labelled in [Board Component Locations](#).

2.1 What's in the box

Todo

List what ships in the box: whether the ePaper panel comes attached, and whether a BL-5C cell and Wi-Fi and LoRa antennas are included.

2.2 Powering the board

Source	Notes
USB Type-C	Powers the board and charges a connected battery at the same time. It also carries the serial console, so one cable is enough for a first boot.
BL-5C battery	A single-cell Li-Ion cell in the Nokia BL-5C form factor. Charge state is reported to software by the on-board fuel gauge.

The board draws far less than a typical single board computer and has an on-board charger with power-path control, so it runs happily from a laptop port. Charging is limited to 430mA with a 45 degrees C cutoff. See [Battery charging and power path](#) for the circuit.

Warning

Check the polarity marked next to the battery connector before fitting a cell. BL-5C cells from different vendors do not all use the same terminal order.

2.3 First boot

Tethered to a PC

The board is powered by the PC over a single USB Type-C cable, which also carries the console. An on-board CP2102N USB-to-UART bridge means no debug probe or separate adapter is needed.

1. Connect a USB Type-C cable between the board and your PC.
2. The board powers on and starts booting.
3. A new serial port appears on your PC. Open it with the settings in [Serial console](#).

Standalone on battery

The board runs from a BL-5C cell with no host attached, and the ePaper display, joystick, buttons, RGB LED and 7-segment digits are the whole interface. This is the mode the board is designed around.

Fit a charged cell, press the power button, and the display will refresh as the board boots. Because the panel is electrophoretic it holds its last image with no power, so a blank or stale screen is not by itself a sign that the board is off.

2.4 Serial console

Setting	Value
Port	The CP2102N bridge on the USB Type-C connector
Baud rate	115200 8N1, no flow control
Linux	/dev/ttyUSB0
macOS	/dev/tty.usbserial-*
Windows	COM*

On Linux and macOS, `tio` or `picocom` are the least troublesome clients:

```
tio /dev/ttyUSB0
```

Todo

Add a trimmed boot log, from power-on to the login prompt, captured on this console.

2.5 Boot media and boot selection

With SELECT released, BeagleBadge boots from its on-board OSPI flash. **Hold SELECT while switching the board on** to boot from a microSD card instead. SELECT and BOOT are the same button. The boot table, and what the OSPI flash is for, are in [Boot Modes](#).

To write an image to a card and boot it, follow [Embedded World 2026 demo image](#).

2.6 Updating the installed software

Todo

Describe updating the installed image once general-purpose BeagleBadge images are on the [Beagle-Board.org distros](#) page: choosing the image, writing it with `flash-latest-image`, and reading the installed version from `/etc/dogtag`.

2.7 Running Zephyr

BeagleBadge has an upstream Zephyr board port. The board target is `beaglebadge/am6213/a53` and applications run on the Cortex-A53 cores.

Copy the built `zephyr.bin` to the first FAT partition of a microSD card, boot the board with SELECT held, interrupt U-Boot, and run:

```
fatload mmc 1:1 0x82000000 zephyr.bin; dcache flush; icache flush; dcache
→off; icache off; go 0x82000000
```

Tip

The [BeagleBadge page in the Zephyr documentation](#) carries the current list of supported peripherals and the build instructions, and is kept up to date with the Zephyr tree rather than with this page.

2.8 Next steps

- [Embedded World 2026 demo image](#): write the demo image and see the board running.
- [Design and Specifications](#): how the hardware works, sheet by sheet.
- [Expansion](#): QWIIC, Grove, mikroBUS and GPIO header pinouts.
- [BeagleBoard.org forum](#): questions and help.

Chapter 3

Design and Specifications

If you want to know how BeagleBadge is designed and the detailed specifications, then this chapter is for you. We are going to provide you a short and crisp overview followed by discussing each hardware design element in detail.

Note

The component details in this chapter are taken from the BeagleBadge v1.0 bill of materials and schematic published in the [BeagleBadge repository](#) (BeagleBadge_V1.0_SCH_260728.pdf and BeagleBadge_BOM.csv). The upstream README notes that specifications are based on the current bill of materials and are subject to change while the design is being finalized.

3.1 Download the schematic

The complete 25-sheet schematic is available as a single PDF:

- BeagleBadge_V1.0_SCH_260728.pdf - BeagleBadge v1.0 schematic, 25 sheets, dated 28 July 2026.

Every sheet of that PDF appears somewhere in this chapter, embedded next to the section that explains it. The table of contents sheet below lists them all.

01. Table of Contents

BeagleBadge v1.0 schematic · page 1 of 25

Schematic: Beaglebadge		Revision History		
SHEET	SHEET NAME	DATE	REVISION	DESCRIPTION
01	Table of Contents	2025/10/14	Rev A	1. Initial
02	Block Diagram			
03	Power Tree			
04	IIC Tree			
05	Power Input 5V	2025/10/20	V0.3	Main modifications: 1. Change the capacitor withstand voltage to 2x or higher. 2. Correct the schematic symbol of the AND gate. 3. Add switch control to the power monitoring ADC. 4. Modify the circuit of RTC_PG and PMIC to reset AM62L. 5. DNI the output capacitor of TPS22965DSGR. 6. Add eMMC circuit. 7. Correct the wake-up signal(WAKEUP0/I1). 8. Change Tag-Connect to SOIC16 Bits. 9. Change button gpios to 3V3 I/Os because connect to SDIOBite 10. DNI I2C singles unpopulated for compatibility touchscreens.
06	RTC ONLY Mode			
07	AM62L PMIC			
08	AM62L Power			
09	AM62L DCAPs			
10	AM62L WKUP & OSC & Reset	2025/10/24	V0.4	1. Replace U9 with OR resistors to switch Low Power mode. 2. Boot and Select function share one button. 3. Replace the Up/Down/Left/Right buttons with a joystick 4. Use the SPI1 to connect U42 (SPI to GPIO) and mikroBUS 5. Correct and add network identification descriptions 6. Adjust some GPIO allocation.
11	AM62L BOOT MODE			
12	AM62L LPDDR4 DEVICE			
13	AM62L OSPI Flash			
14	AM62L Micro SD	2025/10/28	V0.5	1. Added power supply selection for the IMU. 2. Modified the U62 circuit to prevent its input from floating. 3. Added the EXT_WAKEUP0 signal to pin 12 of J29 (SOICbite).
15	AM62L ADC & DSI & OTHER			
16	AM62L USB & HUB	2025/10/29	V0.6	1. Use M23/GPIO0_43/3V3 to reset the USB Hub. 2. Use F22/GPIO0_29/PWM/3V3 to drive the buzzer. 3. The RGB LED has been changed to a smaller package.
17	USB2.0 Type A Host & UART			
18	BM3301 & Sx1262 Module	2025/11/05	V0.7	1. Page8: Correct the VDD80 power supply voltage to 1V8. 2. Page19: The JTAG signals change to 3.3V through a buffer. 3. Page24: The "Other GPIOs" pins shall be changed to 1V8.
19	EEPROM & SOICbite			
20	Button & LEDs			
21	Buzzer & IMU & Light			
22	QWIIIC & MikroBus			
23	ePaper Conn			
24	Other PINs & DSI & Grove	2026/04/25	V1.0	1. Page5:R639 changed to NTC, charging cutoff at 45°C. R341e 2.4K, charging current reduced to 450mA. 2. Page6:Final power mode: RTC ONLY + IO + DDR. Removed main components U6, U8, U10, U39. 3. Page7:Added U88, reworked USB Hub power design. 3V3 and 1V8 only powered when Type-C is connected. 4. Page10:Removed U60, USB Hub now reset directly via GPIO. 5. Page18:Removed U36 LoRa module, added WiFi Power switch button. 6. Page20:Added Power button. D24 replaced with ESD0301L, added 220nF capacitor for ESD protection. 7. Page24:J27: removed AB9/RGMII2_RDO/1V8, added sensor 3V3. 8. Page25:DNP eMMC. 9.General:Minor passives adjustments across schematic.
25	AM62L eMMC			
		2026/07/28	V1.0	1. Mount U36 as required. 2. PCB version number remains unchanged.

seeed studio		https://www.seeedstudio.com	
Title: Beaglebadge		Rev: V1.0	
Doc: A3	Document Number:	01 Table of Contents	Rev: V1.0
Date:	Tuesday, July 28, 2026	Sheet: 1 of 25	

Sheet 01 carries no circuitry. The left half is the schematic's own table of contents, and the right half is the **revision history** of BeagleBadge, from the initial Rev A of 14 October 2025 through to V1.0 of 28 July 2026. It is the quickest way to see what changed between board revisions and why, including the decisions to leave eMMC unpopulated, to merge the boot and select functions onto one button, and to move the "Other GPIOs" pins to 1.8 V.

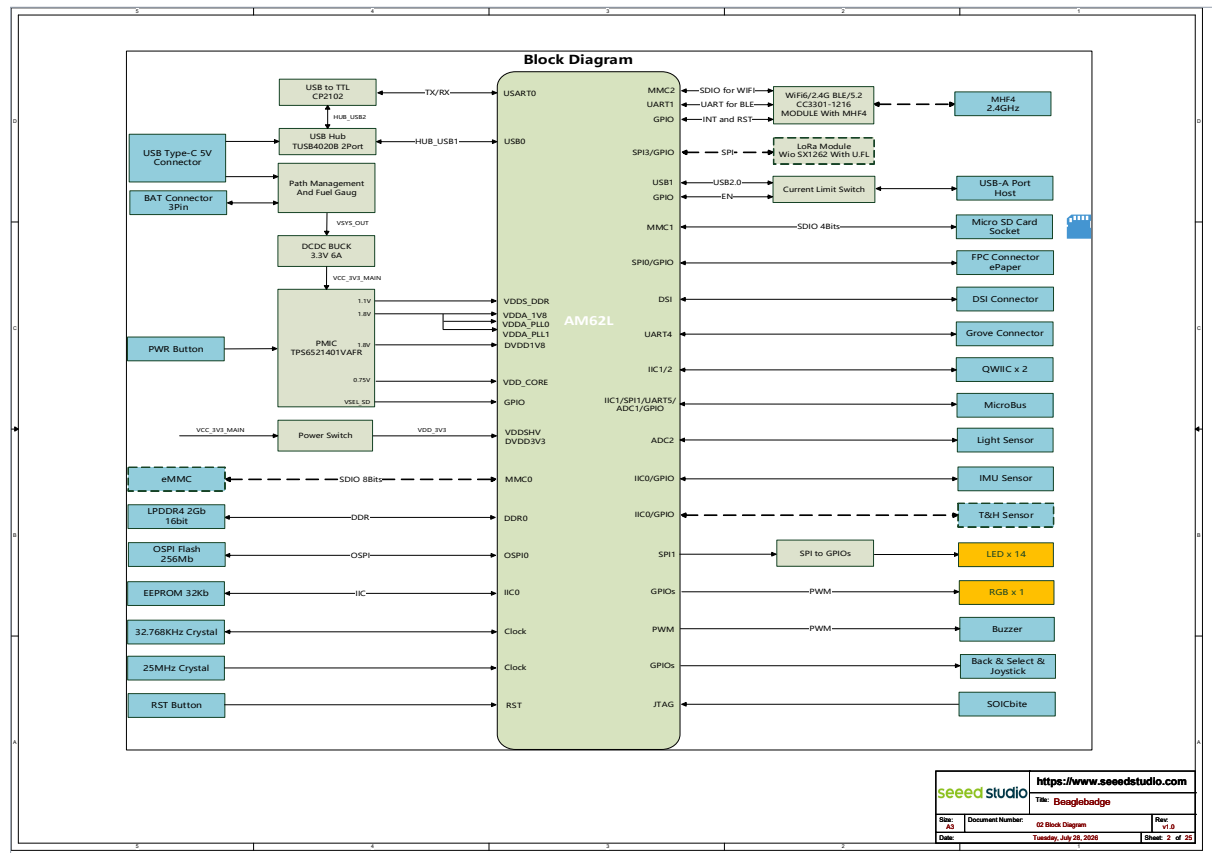
Tip

The schematic sheets in this chapter are interactive: click a highlighted block to read about it, use the toolbar to zoom, and press **F** for a full-screen walk through every annotated sheet. In the PDF build the same highlights are drawn on the vector page and link to the descriptions below it.

3.2 Block Diagram and Overview

02. Block Diagram

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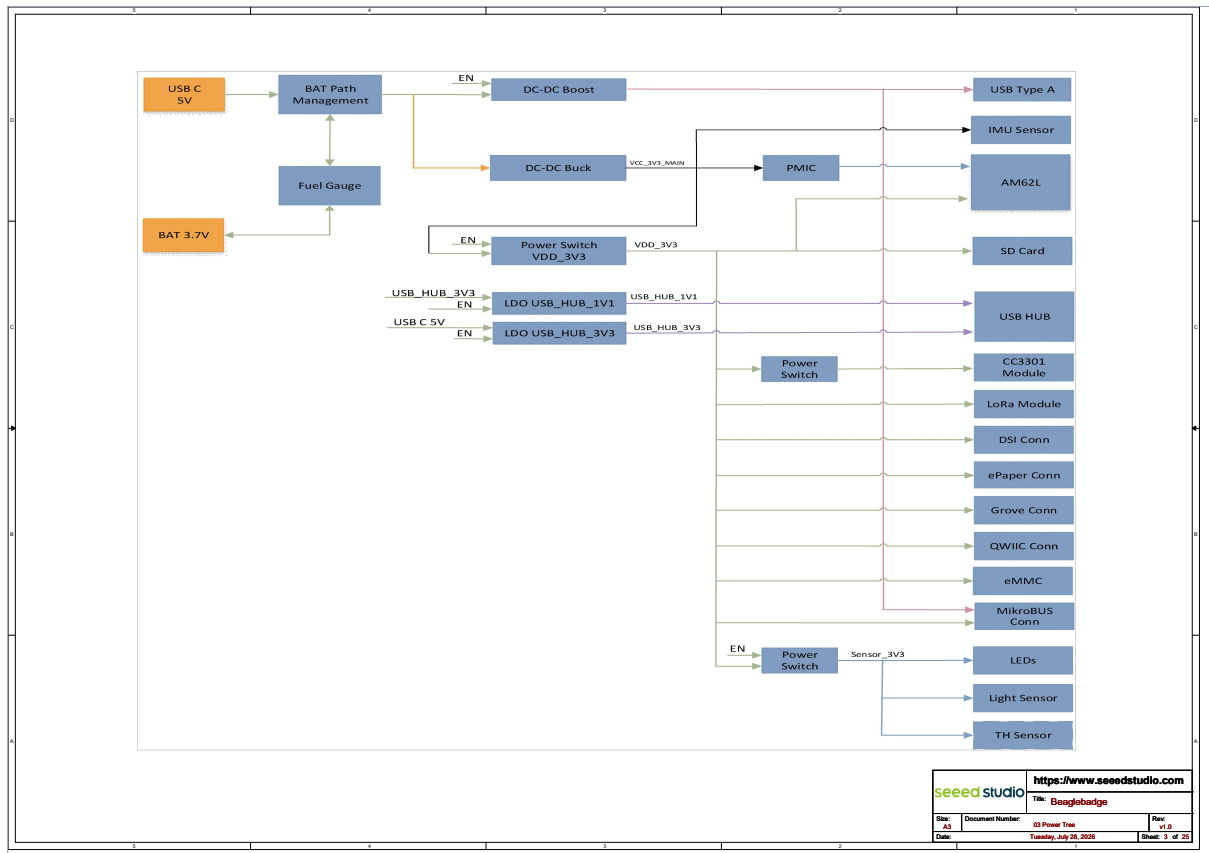


How the SoC, memories, radios, display and expansion connectors relate to one another. Worth reading before any individual sheet.

3.3 Power Tree

03. Power Tree

BeagleBadge v1.0 schematic · page 3 of 25

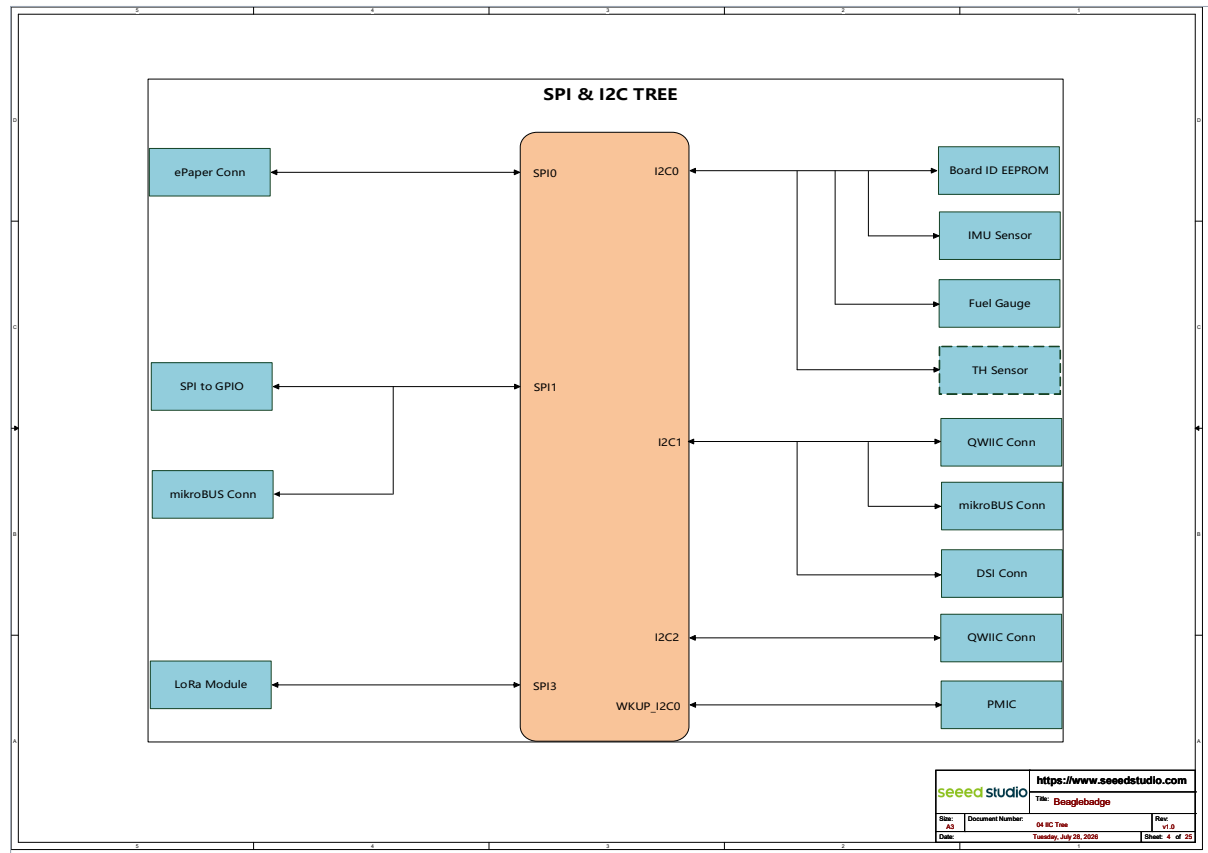


Every rail on the board, from the USB-C and battery inputs down to the SoC supplies, with the regulator that generates each one and the current it can deliver.

3.4 SPI & I2C Tree

04. IIC Tree

BeagleBadge v1.0 schematic · page 4 of 25



Which device sits on which I2C bus, and how the SPI chip selects are allocated. Check here for address clashes before adding a QWIIC, Grove or mikroBUS device.

3.5 System on Chip (SoC)

BeagleBadge is built around the Texas Instruments [AM62L32](#) (AM62L32BOGHAANBR), a low-power member of the K3 Sitara family targeted at IoT, human-machine-interface (HMI) and general-purpose applications where battery life matters as much as compute.

Some of the main characteristics of the device are:

- Dual 64-bit Arm® Cortex®-A53 microprocessor subsystem running at up to 1.25GHz, with 32KB L1 instruction and data caches per core and a shared 256KB L2 cache
- 160KB of shared on-chip SRAM (OCSRAM)
- 16-bit LPDDR4/DDR4 memory interface running at up to 1600MT/s
- Single display output supporting up to 1920x1080 at 60fps over MIPI DSI (4-lane D-PHY) or DPI (24-bit RGB LVCMOS)
- Two USB 2.0 dual-role device subsystems
- eMMC (HS200), SD/SDIO (UHS-I) and OSPI/QSPI storage interfaces
- Eight UARTs, four SPI, five I2C and three McASP audio ports
- One 12-bit ADC with four inputs at 2MSPS

- Multi-voltage configurable GPIO banks (1.8V/3.3V)
- Deep low-power modes including Standby, DeepSleep, RTC+IO+DDR and RTC-only
- 373-pin FCCSP package, 11.9mm x 11.9mm, built on a 16nm process

Tip

The AM62L32 has no separate Cortex-R5F MCU island and no PRU subsystem. If you are coming from BeagleBone class hardware, plan for the Cortex-A53 cores plus the on-chip peripherals to do all the work.

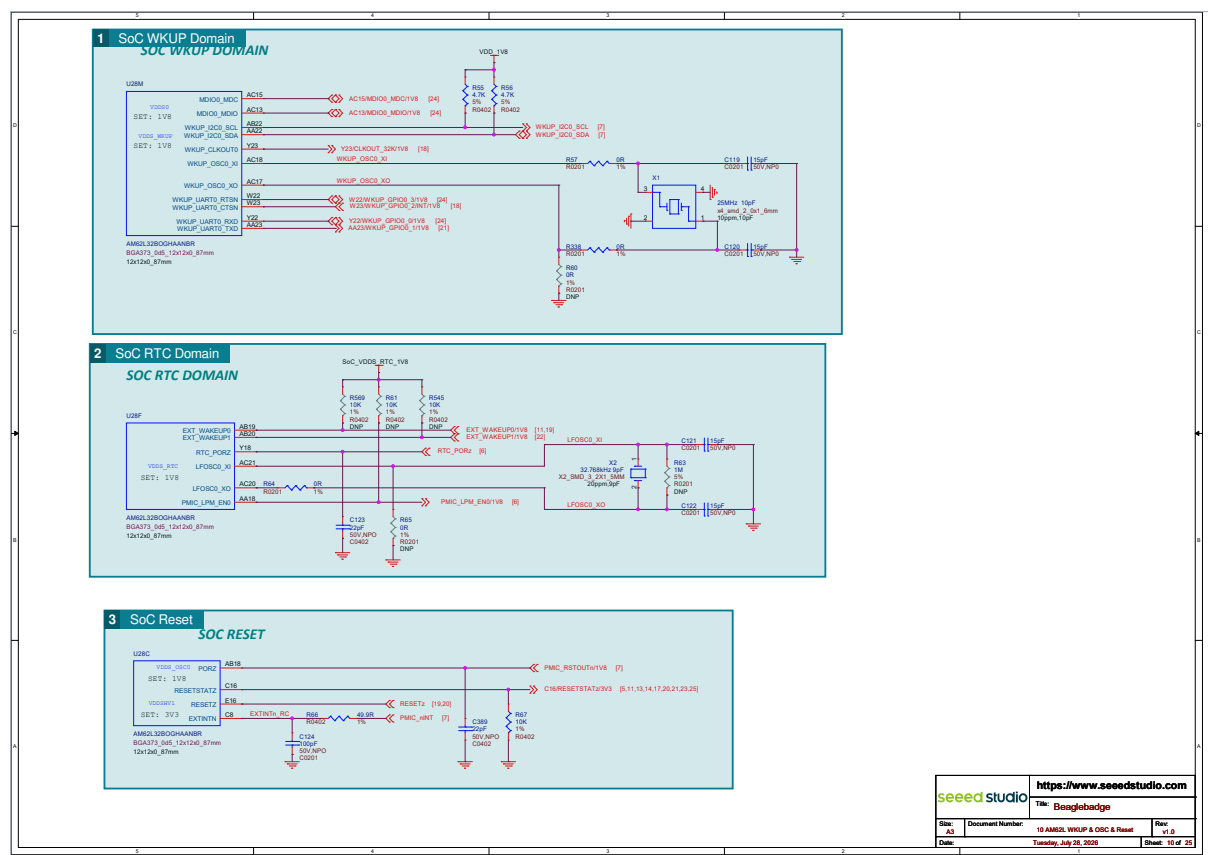
3.5.1 Clocks, wake-up and reset

BeagleBadge runs from two crystals: X1, a 25MHz 10ppm part on WKUP_OSC0, is the main system reference, and X2, a 32.768kHz 20ppm part on LFOSC0, keeps the real-time clock running while the rest of the SoC is powered down.

Reset arrives at the SoC on three pins: PORZ is the cold power-on reset from the PMIC, RESETZ the warm reset from the RESET button, and RESETSTATZ a status output that the rest of the board uses to hold peripherals off until the SoC is out of reset.

10. AM62L WKUP & OSC & Reset

BeagleBadge v1.0 schematic · page 10 of 25



X1 (25MHz) and X2 (32.768kHz), the wake-up and RTC domains, and the three reset entry points into the SoC.

1 SoC WKUP Domain soc U28M X1 C123 C389 R66 R338

The wake-up domain of the AM62L32, the part of the SoC that stays alive in low power modes. It carries WKUP_I2C0 to the PMIC, the WKUP_UART0 pins (reused here as GPIO on the expansion header), WKUP_CLKOUT0 and the MDIO0 pair. X1, a 25 MHz 10 ppm crystal, is the main system oscillator on WKUP_OSC0_XI / WKUP_OSC0_XO.

- ADC0_AIN3 (V21): brought out to the GPIO expansion header, sheet 24

All four are 1.8 V inputs. See [Sensors](#).

2 SoC MCASP and UART soc U28G

The MCASP0 audio serialiser: four data lines AXR0-AXR3 plus transmit and receive clock and frame sync. BeagleBadge fits no audio codec, so these pins are used as 3.3 V GPIO and PWM instead: GPIO0_81, GPIO0_82 and GPIO0_83 drive the RGB LED and the buzzer on sheet 21, and GPIO0_84 goes to the mikroBUS socket.

3 SoC DSI soc U280 R146 R149 R154 C178 C179

The MIPI DSI transmitter: a clock pair and four data lanes on D-PHY, plus DSI0_TXRCALIB with its R146 (499 ohm 1%) calibration resistor. The pairs run to the 22-pin FPC connector on sheet 24. VDDA_1P8_DSI and VDDA_CORE_DSI supply the PHY. See [MIPI DSI](#).

4 SoC Ethernet Interface soc U28L

Both RGMII ports of the AM62L32. **BeagleBadge fits no Ethernet PHY:** all 24 RGMII pins and the MDIO0 pair are repurposed as 1.8 V GPIO and routed to the expansion header on sheet 24. This is why the header silkscreen carries SoC ball names such as Y8, AA6, W8 and AC10 rather than GPIO numbers. See [GPIO expansion header](#).

5 SoC UART, MCAN, I2C, and IOs soc U28A

The general-purpose serial buses, all in the 3.3 V VDDSHV1 bank:

- I2C0: PMIC, fuel gauge, board-ID EEPROM and the IMU
- I2C1: QWIIC connector 1, the mikroBUS socket, the ePaper touch option and the Grove connector
- I2C2: QWIIC connector 2 only, so a module with a fixed address can be used on both QWIIC connectors at once
- UART0: the serial debug console, via the CP2102N bridge on sheet 17
- UART1: the Wi-Fi/BLE module on sheet 18
- UART5: the mikroBUS socket
- SPI0: the ePaper panel on sheet 23
- MCAN0: not used on this board

GPIO0_95 (Right) and GPIO0_104 (BACK) are joystick and button inputs.

3.5.3 Boot Modes

The AM62L32 reads its 16 SYS_BOOTMODE strap pins at power-on and takes a primary and a backup boot device from them. On BeagleBadge the straps are set by resistors, except for the bits that the **SELECT/BOOT** button overrides.

Table 3.1: Boot modes

At power-on	Primary boot	Backup boot	Used for
SELECT released	OSPI NOR flash	UART	Normal start-up from the boot chain in flash
SELECT held	microSD card	USB DFU	Booting an image from a card

If the primary device holds no valid boot image, the ROM moves on to the backup device. With SELECT held, a card that is missing or not bootable leaves the board waiting as a USB DFU device rather than falling back to the OSPI flash.

What the OSPI flash is for

With the boot chain in OSPI:

- ## 11. AM62L BOOT MODE

1 Boot strap bus switches

2 SoC GPMC / boot pins

3 Boot mode strap resistors (BMODE 0-15)

4 Boot mode truth tables

5 Wake-up gates

1 Boot strap bus switches soc U73 U74 C482 C481 R614

3.5. System on Chip (SoC)

at boot.

2 SoC GPMC / boot pins soc U28H R321 R322 R323 R517 R518 R519 R551

Part H of the AM62L symbol: the GPMC0 bank whose pins double as SYS_BOOTMODE[15:0] straps and, after boot, as joystick, button, SPI1/SPI3 and UART4 GPIOs (3.3 V domain).

3 Boot mode strap resistors (BMODE 0-15) soc R69 R83 R88 R102 D6 D52 D49

Each SYS_BOOTMODE_x line has a 10 kΩ pull-up and 100 kΩ pull-down footprint. The populated set selects the default configuration. D6/D52/D49 let the **Select/BOOT button** override bits 3, 6 and 10: released → *OSPI CS0 boot, UART backup*. Pressed → *SD-card FS boot, USB DFU backup*. See [Boot Modes](#).

4 Boot mode truth tables soc

Reference tables printed on the sheet: the 16-bit SYS_BOOTMODE word for *OSPI* → *UART* vs *SD card* → *USB*, and the PLL / primary / backup boot decoding for the button-released and button-pressed cases.

5 Wake-up gates soc U44 U72 C291 C479 R529 R598

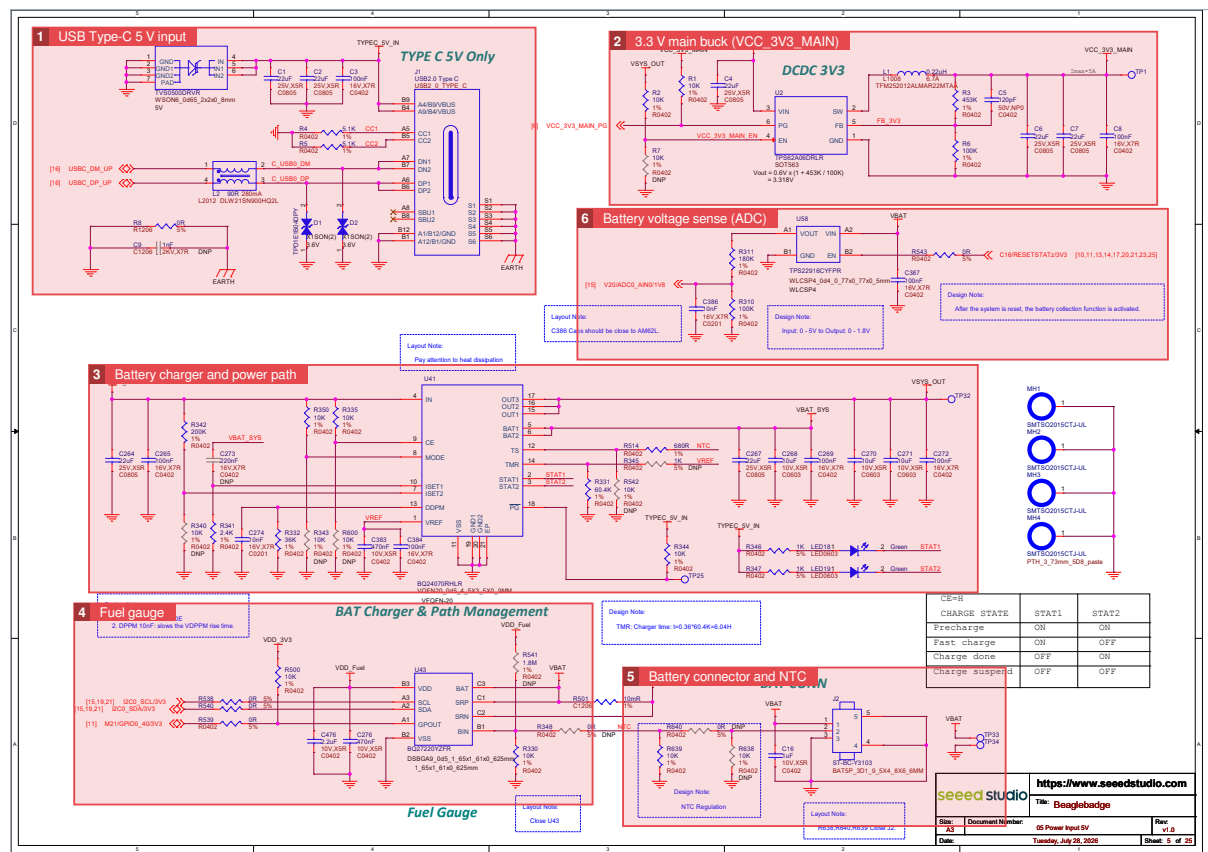
U44 gates SYS_BOOTMODE6 and U72 (SN74LVC1G17) turns Joystick_Press or Select into EXT_WAKEUP0/1V8, either button wakes the system from sleep.

3.6 Power Management

BeagleBadge is designed to run from a single-cell lithium battery or from USB Type-C, with automatic switchover between the two and battery capacity reporting over I2C. To fully understand the power tree, see [Power Tree](#).

05. Power Input 5V

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The Type-C input and its protection, the 3.3V main buck, the charger with its power-path control, and the fuel gauge that reports state of charge over I2C.

1 USB Type-C 5 V input POWER J1 U1 L2 D1 D2 R4 R5 C1 C2 C3 R8 C9 [TVS0500 datasheet](#)

The Type-C receptacle J1 is wired for **5 V power and USB 2.0 data only** (no alternate modes, no Power Delivery). R4/R5 (5.1 kΩ) on CC1/CC2 advertise a UFP sink so a Type-C source will supply 5 V. U1 (TVS0500DRVR) clamps surges on TYPEC_5V_IN, L2 is a 90 Ω common-mode choke on the data pair and D1/D2 add ESD protection. The data pair goes to the USB hub upstream port (see [USB](#)).

2 3.3 V main buck (VCC_3V3_MAIN) POWER U2 L1 R3 R6 C5 C6 C7 C8 TP1 [TPS62A06 datasheet](#)

U2 (TPS62A06DRLR, 6 A synchronous buck) generates VCC_3V3_MAIN, the always-on rail feeding the PMIC, load switches and the rest of the board. The feedback divider R3/R6 (453 kΩ / 100 kΩ) sets $V_{out} = 0.6 \text{ V} \times (1 + 453/100) = 3.318 \text{ V}$. VCC_3V3_MAIN_EN gates the converter and the power-good output goes to the RTC-mode logic on sheet 6. See [Rails, converters and load switches](#).

3 Battery charger and power path POWER U41 R341 R342 R331 R542 LED181 LED191 [BQ24070 datasheet](#)

U41 (BQ24070RHLLR) is a single-cell Li-Ion linear charger with **dynamic power-path management**: the system runs from VSYS_OUT while the battery charges, and switches to the battery seamlessly when USB-C is removed. In v1.0 R341 was changed to 2.4 kΩ, reducing the fast-charge current to about **430 mA**, and the timer resistor sets a 6 h safety timer. STAT1/STAT2 drive the two green charge-status LEDs (LED181, LED191) and the table on the sheet lists the LED states. See [Battery charging and power path](#).

4 Fuel gauge POWER U43 R500 R538 R540 R541 R330 R501 C476 C276 [BQ27220 datasheet](#)

U43 (BQ27220YZFR) measures charge flowing through the 10 mΩ sense resistor R501 and reports state of charge over I2C0 (3.3 V). GPOUT is routed to M21/GPIO0_40 for battery-low interrupts. The gauge is powered from VDD_Fuel, derived directly from VBAT so it keeps counting while the SoC sleeps.

5 Battery connector and NTC POWER J2 R639 R640 R638 C16

J2 (ST-BC-Y3103) has three spring contacts for a **Nokia BL-5C** form-factor cell, held to the board by two support legs. R639 was changed to an NTC in v1.0 so the charger suspends charging above about **45 °C**. R638/R640 scale the thermistor into the charger's TS window. Keep R638, R639 and R640 close to J2.

6 Battery voltage sense (ADC) POWER U58 R311 R310 C386 C387 R543 [TPS22916 datasheet](#)

R311/R310 (180 kΩ / 100 kΩ) divide 0-5 V on VBAT down to the 0-1.8 V range of ADC0_AIN0. The divider is switched by U58 (TPS22916) and enabled from RESETSTATz so it draws no battery current until the SoC is out of reset. C386 should be placed next to the AM62L ADC pin.

3.6.1 PMIC

The main rails for the SoC and DDR are generated by a Texas Instruments [TPS6521401](#) (TPS6521401VAFR) power management IC in a QFN-24 package, which integrates three DC/DC converters and two LDOs.

It runs from VCC_3V3_MAIN, the 3.3V rail generated by the U2 buck converter, and uses TI's default configuration for the AM62L, described in the [TPS6521401 technical reference manual](#).

Table 3.2: PMIC outputs

Output	Rail	Supplies
BUCK1	VDD_CORE, 0.75V, 2A	SoC core
BUCK2	VDD_1V8, 1.8V, 1A	SoC 1.8V and RTC I/O, OSPI flash, LPDDR4 VDD1, Wi-Fi 1.8V
BUCK3	VDD_LPDDR4, 1.1V, 1A	LPDDR4 VDD2 and VDDQ, SoC VDD2, SoC VDD3, SoC VDD4
LDO1	VDDA_1V8, 1.8V, 0.3A	SoC 1.8V analog supplies
LDO2	PMIC_VDD_RTC, 0.75V, 0.5A	SoC RTC core

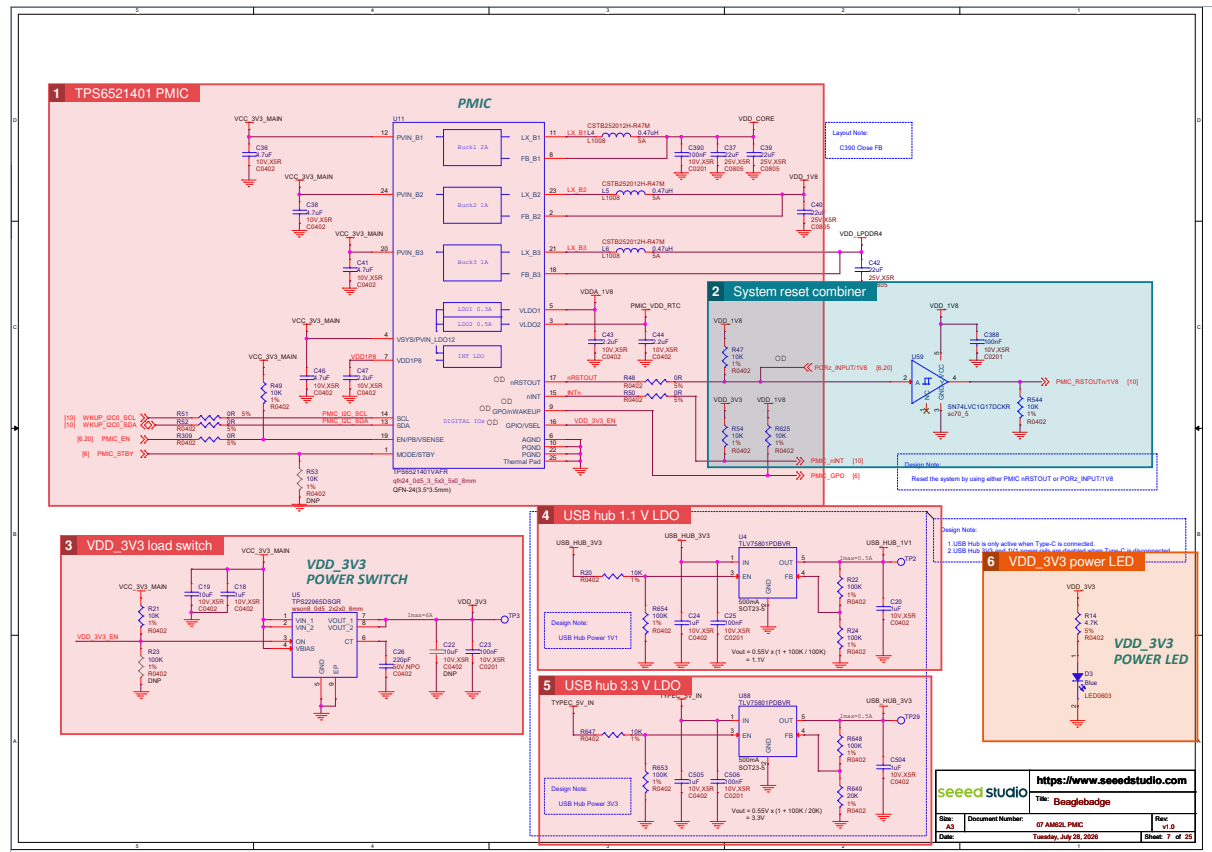
At power-up the PMIC brings the rails up in this order:

1. GPIO enables the VDD_3V3 load switch.
2. BUCK2, LDO1 and LDO2.
3. BUCK3, and GPO signals RTC power-good to RTC_PORz.
4. BUCK1.
5. nRSTOUT releases the SoC from reset, about 19ms after the PMIC is enabled.

In standby, which is the RTC + IO + DDR low power mode, BUCK1 and LDO1 turn off and nRSTOUT holds the SoC in reset. The other rails stay on so the LPDDR4 keeps its contents. See [Low power modes](#).

07. AM62L PMIC

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The TPS6521401 PMIC and the load switches and LDOs derived from it. Revision V1.0 reworked this sheet so that the 3.3V and 1.8V hub rails are powered only while Type-C is connected.

1 TPS6521401 PMIC POWER U11 L4 L5 L6 C37 C39 C40 C42 C43 C44 TPS65214 datasheet

U11 (TPS6521401VAFR) produces the SoC core rails from VCC_3V3_MAIN:

- **Buck1** (2 A) → VDD_CORE (0.75 V)
- **Buck2** (1 A) → VDD_1V8
- **Buck3** (1 A) → VDD_LPDDR4 (1.1 V)
- **LDO1** (0.3 A) → VDDA_1V8, **LDO2** (0.5 A) → PMIC_VDD_RTC

The PMIC is controlled over WKUP_I2C0 and its nRSTOUT/nINT outputs go to the SoC reset and wake-up domain. See [PMIC](#).

2 System reset combiner soc U59 R47 R54 R625 R544 C388

U59 (SN74LVC1G17) buffers PORz_INPUT/1V8 into PMIC_RSTOUTn/1V8 so the system can be reset either by the PMIC nRSTOUT or by the external reset input (RESET button / SOICbite). The pull-ups R47,

R54 and R625 reference the signals to their respective 1.8 V and 3.3 V domains.

3 VDD_3V3 load switch POWER U5 R21 R23 C19 C18 C22 C23 TP3 [TPS22965 datasheet](#)

U5 (TPS22965DSGR, 6 A, 16 mΩ) gates VDD_3V3 from VCC_3V3_MAIN. It is enabled by VDD_3V3_EN from the PMIC GPIO so that the peripheral 3.3 V domain is sequenced after the core rails. C22 is DNI per the v0.3 change list.

4 USB hub 1.1 V LDO POWER U4 R20 R654 R22 R24 C24 C25 C20 TP2 [TLV758P datasheet](#)

U4 (TLV75801PDBVR, 500 mA adjustable LDO) creates USB_HUB_1V1 for the TUSB4020B core. R22/R24 (100 kΩ / 100 kΩ) set $0.55 \text{ V} \times 2 = 1.1 \text{ V}$. The LDO is enabled from USB_HUB_3V3 so both hub rails follow the Type-C presence.

5 USB hub 3.3 V LDO POWER U88 R647 R653 R648 R649 C505 C506 C504 TP29 [TLV758P datasheet](#)

U88 (TLV75801PDBVR) regulates TYPEC_5V_IN to USB_HUB_3V3 with R648/R649 (100 kΩ / 20 kΩ) $\rightarrow 0.55 \text{ V} \times 6 = 3.3 \text{ V}$. Because its input is the Type-C 5 V rail, the hub is **only powered while a USB-C cable is connected**. On battery the hub and its 1.1 V LDO are off (design note on the sheet, added in v1.0).

6 VDD_3V3 power LED USER INTERFACE D3 R14

Blue 0603 LED D3 with 4.7 kΩ series resistor R14 indicates that the switched VDD_3V3 rail is up, i.e. the board has finished power sequencing.

3.6.2 Battery charging and power path

Table 3.3: BeagleBadge battery subsystem

Function	Device	Notes
Charger and power path	BQ24070 (BQ24070RHLLR)	Single-cell Li-Ion/Li-Po linear charger with dynamic power-path management, so the board can run from USB while the battery charges
Fuel gauge	BQ27220 (BQ27220YZFR)	I2C battery fuel gauge for Li-Ion and Li-Polymer cells, reports state of charge to software
Battery connector	J2, ST-BC-Y3103	Three spring contacts for a Nokia BL-5C form-factor cell, held to the board by two support legs

Revision V1.0 set the charge current with R341 (2.4K) to **430mA**, and changed R639 to an NTC thermistor so that charging stops at **45 degrees C**. At 430mA a typical 1000mAh BL-5C cell takes roughly three hours to charge.

Todo

Add the J2 contact order and the charger's input current limit, from [schematic sheet 5](#).

3.6.3 Rails, converters and load switches

Beyond the PMIC, discrete converters generate the main 3.3V input and the 5V and USB hub rails.

Table 3.4: Converters

Part	Output	Notes
U2 TPS62A06, 6A buck	VCC_3V3_MAIN, 3.3V	Always on, feeds the PMIC and VDD_3V3
U23 LMR62014, boost	BOOST_5V0, about 4.95V, 600mA	Type-A port, and the mikroBUS 5V pin limited to 0.1A
U88 TLV75801, LDO	USB_HUB_3V3	From USB-C 5V, so on only while USB-C is connected
U4 TLV75801, LDO	USB_HUB_1V1	Follows USB_HUB_3V3

VDDSHV4 banks are the multi-voltage I/O domains that make the 1.8 V and 3.3 V pin groups possible. Analogue rails (VDDA_1P8_USB, VDDA_3P3_USB, VDDA_CORE_USB, VDDA_1P8_DSI, VDDA_CORE_DSI, VDDA_ADC, VDDA_PLL0/1) are broken out separately so each can be filtered on its own. VPP is the one-time-programmable efuse supply and is tied to 1.8 V through J16, a header left unpopulated on production boards.

2 SoC VSS (GND) POWER U28Q

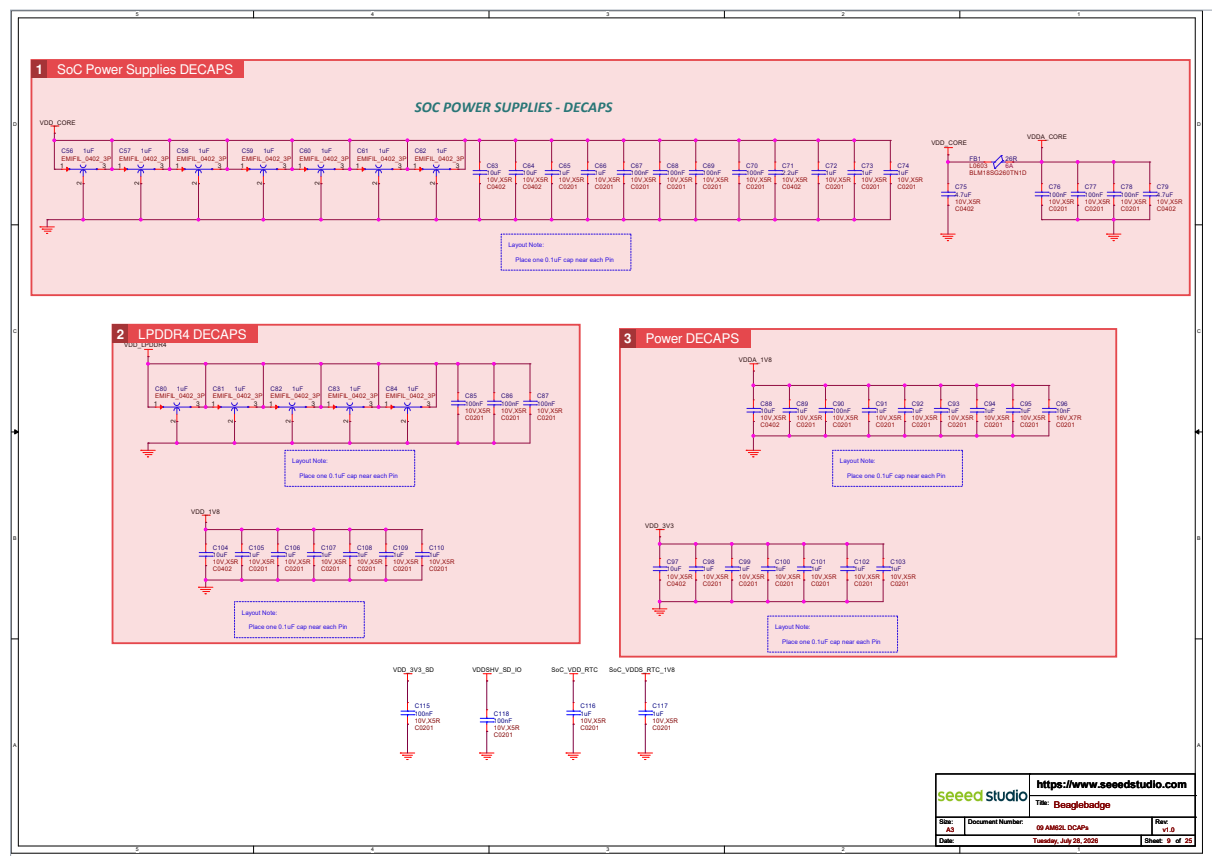
The ground return for the SoC. The AM62L32 brings VSS out on roughly a hundred balls spread across the 373-ball array, all tied to the board ground plane. The dense ball count is a thermal and return-path requirement, not an electrical one: it keeps the impedance of the return low under the DDR and USB interfaces.

3 SoC power caps POWER C55 C111 C112 C113

Bulk and reservoir capacitance for the SoC internal regulators. CAP_VDDS_MMC0, CAP_VDDS_MMC1, CAP_VDDS_MMC2, CAP_VDDS_GPMC, CAP_VDDS_GENERAL1 and CAP_VDDSHV_MMC are not supply inputs: they are the external capacitors the SoC's on-die LDOs need to stay stable. They must sit close to their balls.

09. AM62L DCAPS

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Decoupling for every SoC supply ball. The repeated layout note, one 0.1uF capacitor next to each pin, is the constraint that drives much of the board's bottom-side component placement.

1 SoC Power Supplies DECAPS POWER

High-frequency decoupling for the SoC supply rails. Every supply ball gets its own 0.1 uF capacitor, as the repeated layout note on the sheet requires, backed by bulk 4.7 uF and 10 uF parts per rail. The EMIFIL three-terminal feedthrough capacitors (C56-C62, C80-C84) are used where a plain two-terminal part would not have enough self-resonant bandwidth.

2 LPDDR4 DECAPS POWER

Decoupling for the VDD_LPDDR4 rail feeding the SoC side of the memory interface. LPDDR4 switching current is both large and fast, so this rail gets its own capacitor bank rather than sharing with the core supply. See [256MB LPDDR4](#).

3 Power DECAPS POWER FB1

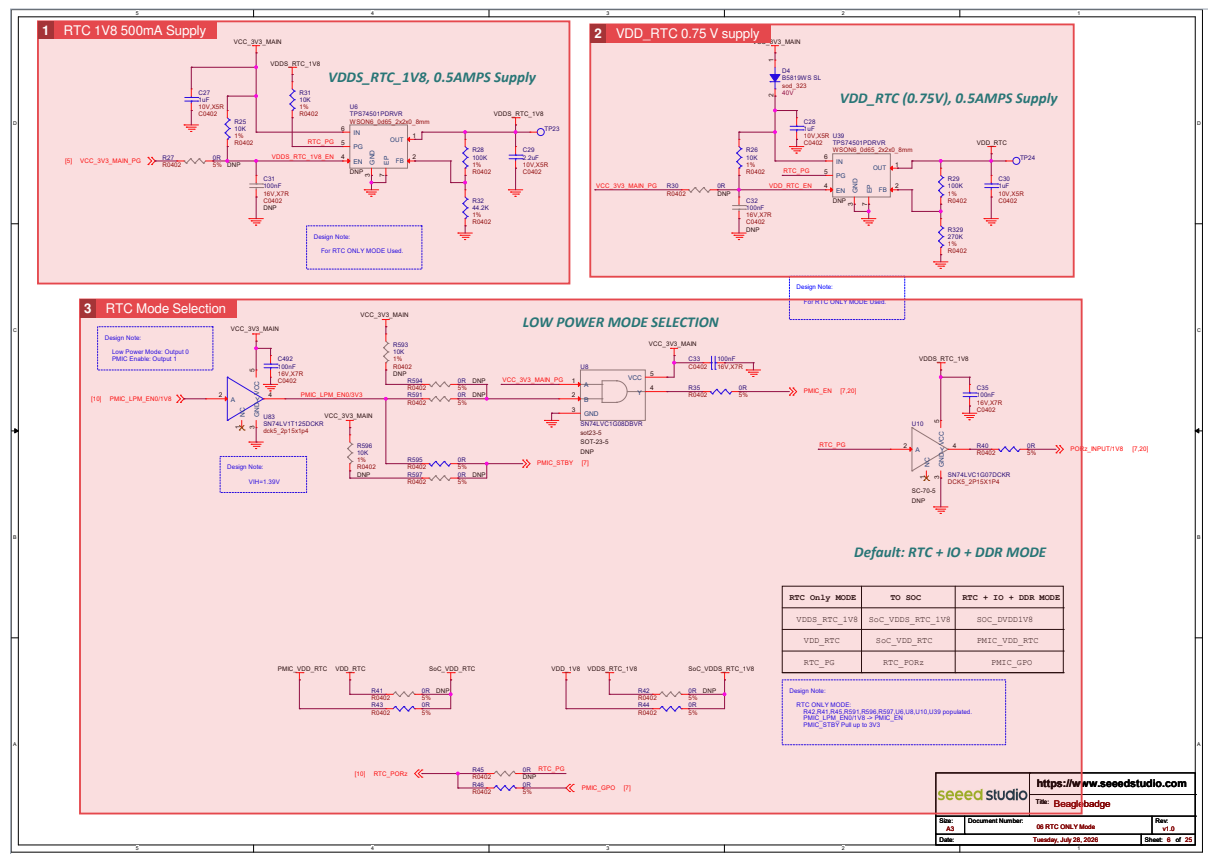
Decoupling for the remaining board rails at the SoC: VDD_3V3, VDD_3V3_SD, VDD_1V8, VDDA_1V8, VDDSHV_SD_IO and the RTC pair SoC_VDD_RTC / SoC_VDDS_RTC_1V8. FB1 (26 ohm, 6 A ferrite bead) isolates the analogue 1.8 V rail from switching noise on the digital one.

3.6.5 Low power modes

BeagleBadge is a battery-powered design, so the schematic provides for more than one sleep depth. Revision V1.0 settled on RTC ONLY + IO + DDR as the final power mode and removed the parts that the deeper RTC ONLY mode would have needed.

06. RTC ONLY Mode

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2 VDD_RTC 0.75 V supply POWER U39 [TPS74501 datasheet](#)

U39, a TPS74501PDRVR LDO for the 0.75 V VDD_RTC rail (up to 0.5 A), enabled by VDD_RTC_EN. **Not populated**, for the same reason as U6 beside it.

3 RTC Mode Selection POWER R41 R42 R45 R591 R596 R597 U6 U8 U10 U39 U83

Selects which low-power mode the board supports. The sheet offers two:

- RTC + IO + DDR: **the default**, and how the board ships. The components in the two supply blocks on this sheet are left unpopulated and the PMIC supplies VDD_RTC and VDDS_RTC_1V8 directly.
- RTC ONLY: the deepest mode. It requires R41, R42, R45, R591, R596, R597, U6, U8, U10 and U39 to be populated, PMIC_LPM_EN0/1V8 routed to PMIC_EN, and PMIC_STBY pulled up to 3.3 V.

Revision V1.0 settled on RTC ONLY + IO + DDR as the final power mode and removed U6, U8, U10 and U39 from the build.

3.7 Memory, Media and Storage

3.7.1 256MB LPDDR4

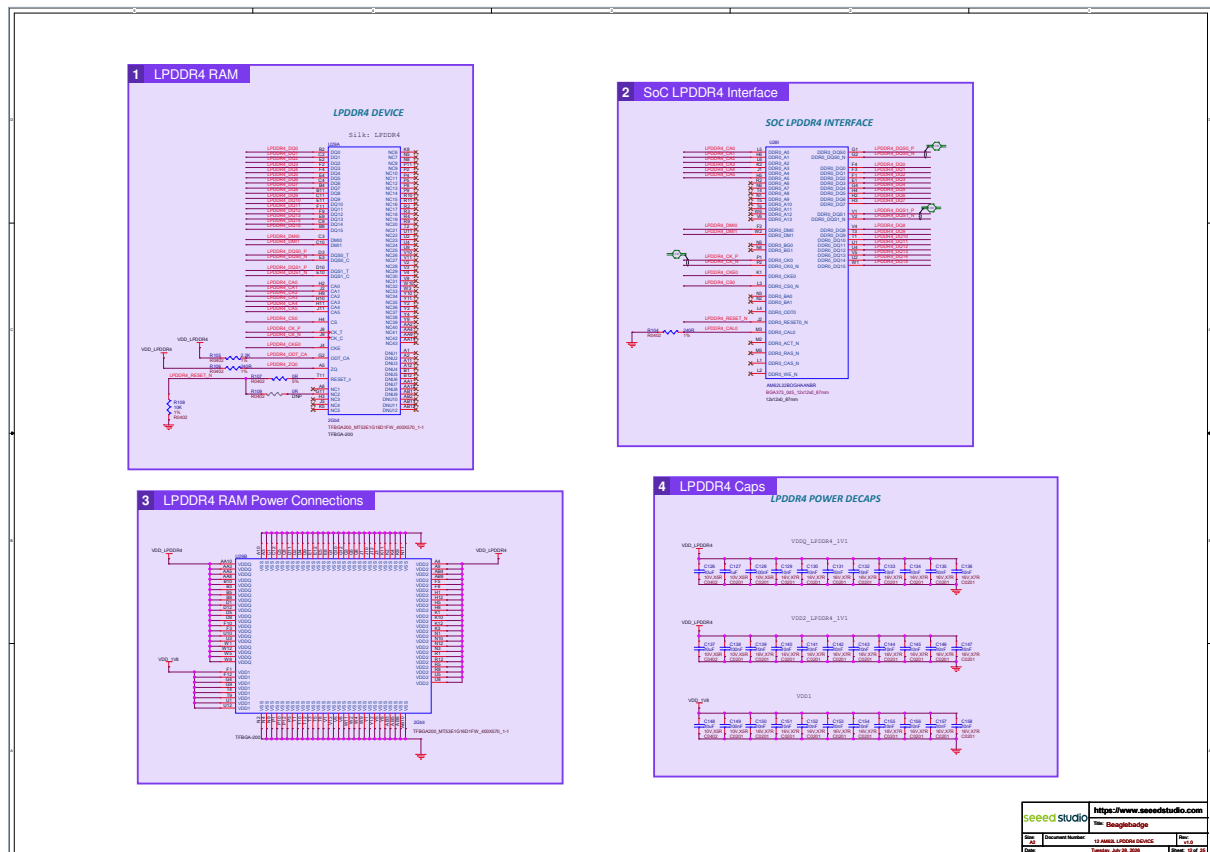
BeagleBadge v1.0 has **256MB** of system memory on a 16-bit bus. It comes from a single ISSI IS43LQ16128A-062BLI LPDDR4 device in a 200-ball FBGA package, a 2Gb part organised as 128M x 16.

Important

Some retail listings describe this as “2GB LPDDR4”. That is a unit error: 2 **gigabit** is 256 **megabytes**. The upstream BeagleBadge README, the Zephyr board documentation and the bill of materials all agree on 256MB.

12. AM62L LPDDR4 DEVICE

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The 2Gb device and the 16-bit SoC interface, with the 240 ohm ZQ calibration references and the routing impedance targets noted on the sheet.

1 LPDDR4 RAM MEMORY & STORAGE U29A U29B [IS43LQ16128A datasheet](#)

U29, the IS43LQ16128A-062BLI LPDDR4 device in a 200-ball TFBGA. It provides **256 MB** of system memory on a 16-bit bus at up to 1600 MT/s, from a 2 Gb part organised as 128M x 16. Note the large number of NC and DNU balls: the footprint is the standard LPDDR4 package, and a wider or denser device could drop into it. See [256MB LPDDR4](#).

2 SoC LPDDR4 Interface MEMORY & STORAGE U28I R104 R105 R106 R108

The SoC side of the memory bus: a 16-bit LPDDR4 interface with DDR0_DQ0-DQ15, two data strobe pairs, two data masks, a 14-bit address bus, bank and command signals. R104 and R106 (240 ohm 1%) are the ZQ calibration references and R105 (2.2 k) the DDR0_CAL0 reference. See [256MB LPDDR4](#).

3 LPDDR4 RAM Power Connections MEMORY & STORAGE

Supply balls of the LPDDR4 device. LPDDR4 needs three separate rails: VDD1 (1.8 V) for the internal regulator, VDD2 (1.1 V) for the core array and VDDQ (1.1 V) for the I/O drivers. VDD2_LPDDR4_1V1 and VDDQ_LPDDR4_1V1 come from the PMIC. VDD1 shares the board VDD_1V8 rail.

4 LPDDR4 Caps MEMORY & STORAGE

Decoupling for the memory device, placed on the underside directly beneath the ball field. The bank is mostly 10 nF 0201 parts so that each can sit as close to its ball as possible, with 10 uF and 100 nF bulk parts per rail. The silkscreen marking for this block is LPDDR4, and the impedance annotations on the sheet (80E, 66E) are the routing targets for the data and command/address groups.

3.7.2 Storage

Table 3.6: On-board non-volatile storage

Type	Device	Capacity
OSPI NOR flash	ISSI IS25WX256-JHLE	256Mb (32MB), FBGA-24
EEPROM	FMD FT24C32A-ELRT	32Kb, I2C, SOT23-5
eMMC	Footprint only	Not populated on v1.0
Removable	ST-TF-003J card holder	microSD socket, 9-pin

The EEPROM sits on I2C0 and follows the BeagleBoard.org convention of holding the board identity, so software can detect which board it is running on. It is write-protected by a pull-up on WP. Pull test point TP16 low to write it.

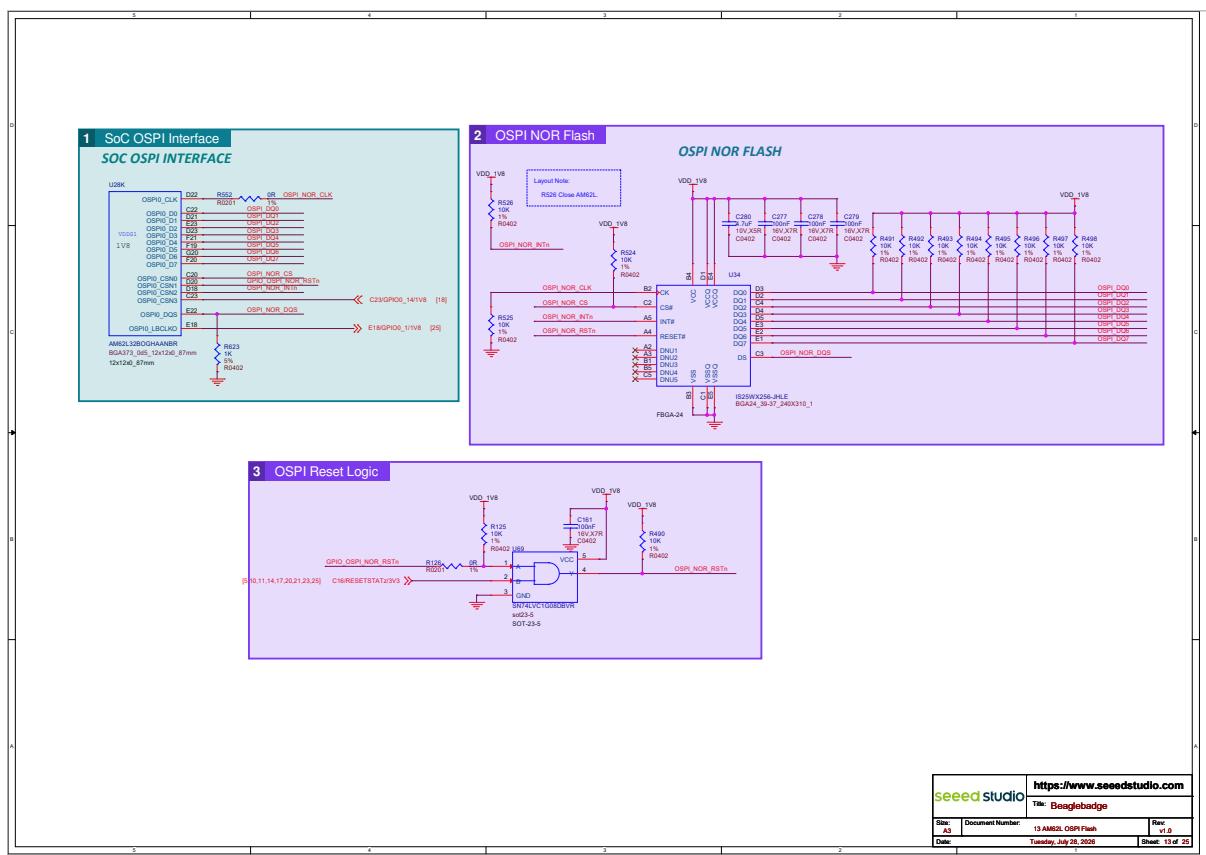
Todo

Add the EEPROM's I2C address and the data format written at manufacturing, in the style of the AI-64 bbai64-expansion EEPROM section.

OSPI NOR flash

13. AM62L OSPI Flash

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bank. Only CSN0 is used, for the NOR flash beside it.

2 OSPI NOR Flash MEMORY & STORAGE U34 C161 C277 C278 C279 C280 IS25WX256 datasheet

U34, an ISSI IS25WX256-JHLE octal NOR flash in a 24-ball FBGA: **256 Mb (32 MB)**, 1.8 V. It is the only non-removable boot medium on the board and holds the boot chain. See [What the OSPI flash is for](#).

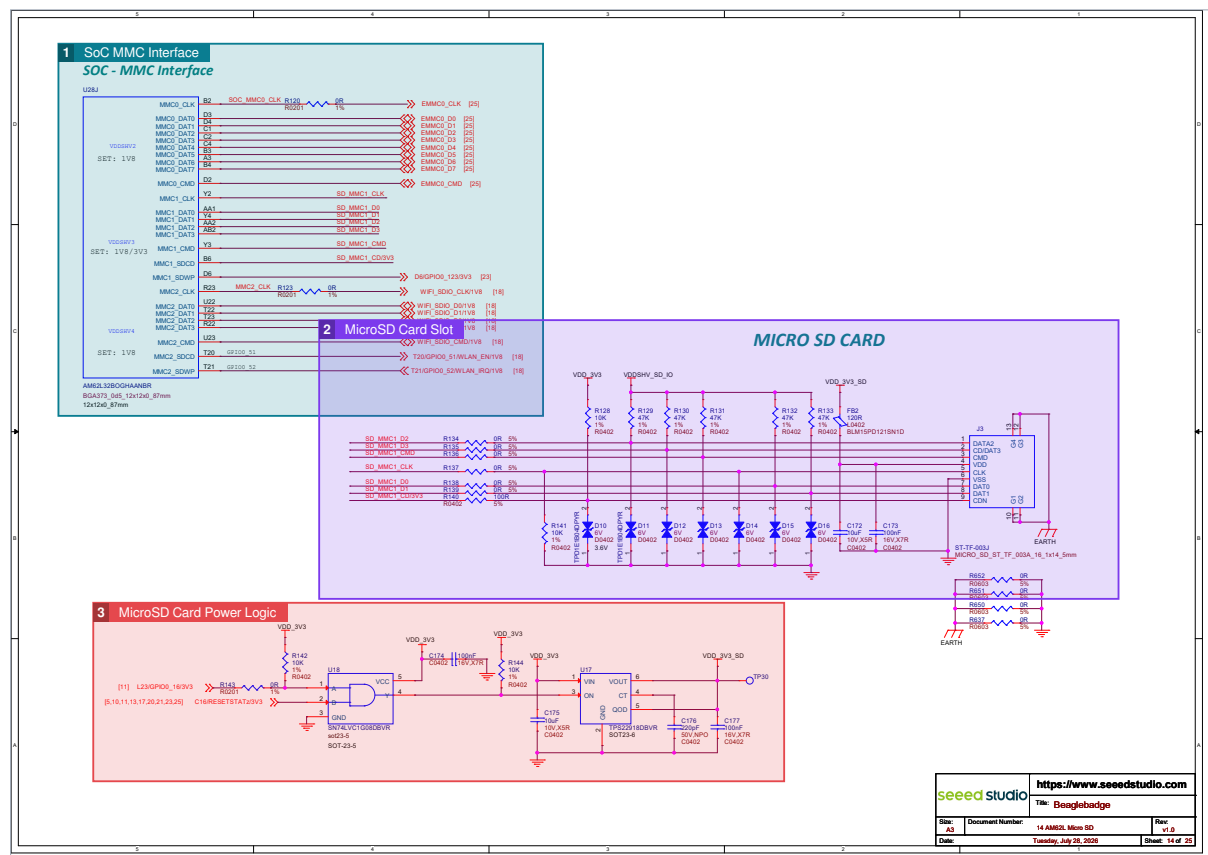
3 OSPI Reset Logic MEMORY & STORAGE U69 R526 R525 R524 R623

U69 (SN74LVC1G08 AND gate) combines the SoC GPIO_OSPI_NOR_RSTn with the board-wide RE-SETSTATz so the flash is held in reset until the SoC itself is out of reset. Without this the flash could be mid-transaction when the SoC restarts. The layout note asks for R526 to be placed close to the SoC.

microSD

14. AM62L Micro SD

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3 MicroSD Card Power Logic POWER U17 U18 R142 R144 C172 C175 TPS22918 datasheet

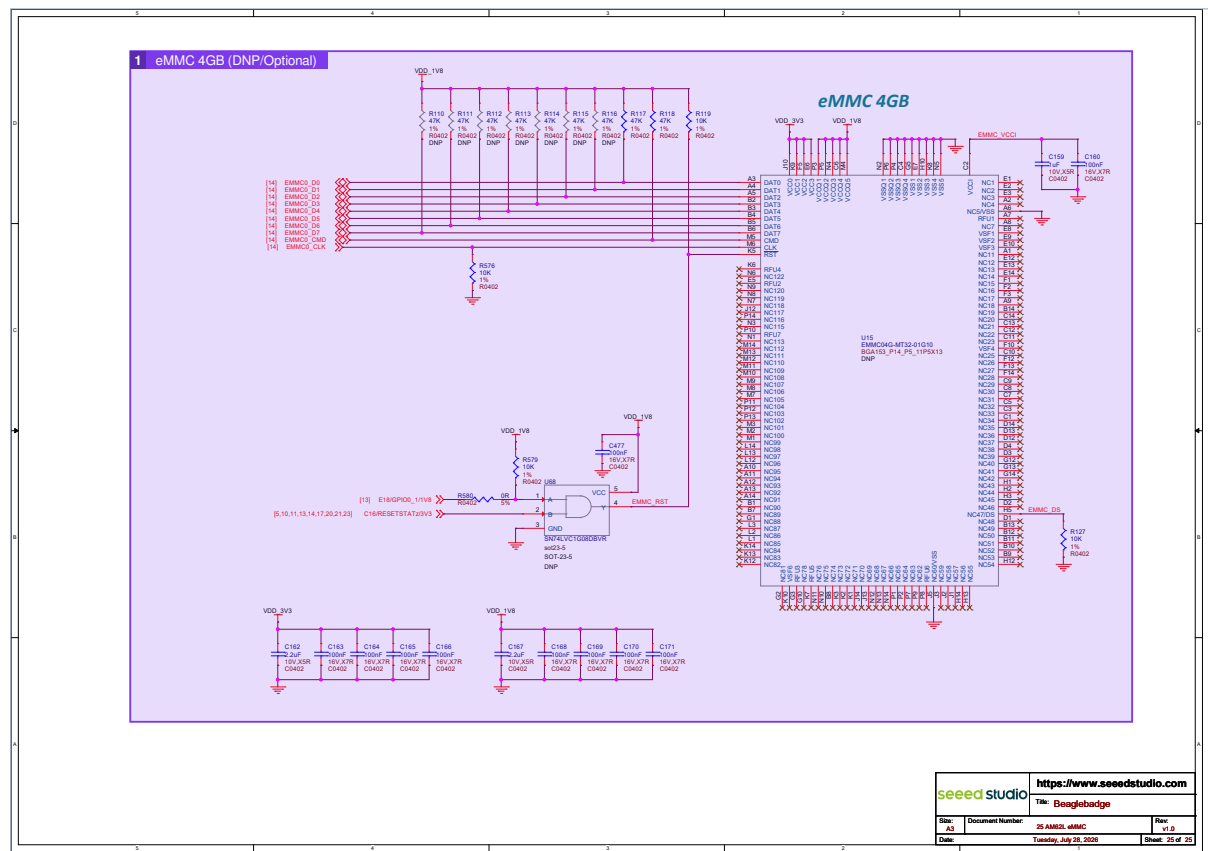
U17 (TPS22918DBVR load switch) gates VDD_3V3_SD to the card so software can power-cycle it, which is how an SD card is recovered from a hung state. U18 (SN74LVC1G08) gates the enable with RESETSTATz so the card stays unpowered until the SoC is out of reset. VDDSHV_SD_IO follows the card rail so the I/O bank tracks whatever voltage the card is running at, which is what allows both 3.3 V and 1.8 V UHS-I signalling.

eMMC footprint

The SoC MMC0 bus is routed to a footprint for a 4GB eMMC device. No eMMC is fitted on v1.0.

25. AM62L eMMC

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Wi-Fi uses the SoC MMC2 SDIO interface and Bluetooth uses UART1. The module's 3.3V and 1.8V supplies both pass through load switches that are **off by default**, so the radio stays powered down until software drives AB9/GPIO0_75 high. See [Rails, converters and load switches](#).

Table 3.7: BM3301-1216 module summary

Parameter	Value
Wireless IC	TI CC3301 SimpleLink companion IC
Wi-Fi	802.11ax (Wi-Fi 6), 2.4GHz only
Bluetooth	Bluetooth Low Energy (BLE) 5.4
Throughput	Application throughput up to 50 Mbps
Antenna connector	IPEX Gen 4 / MHF4 (ECT818000500)
Certification	Certified to FCC/CE intentional radiator emission requirements

Note

5GHz Wi-Fi bands and Bluetooth Classic are **not** supported by the CC3301. Only the 2.4GHz band and Bluetooth Low Energy are available.

3.8.2 LoRa

Long-range sub-GHz connectivity is provided by a Seeed Studio [Wio-SX1262](#) module (U36), built on the Semtech SX1262 transceiver and connected on SPI3, with a u.FL antenna connector. It is the hardware behind the Meshtastic support described in [Demos and Tutorials](#).

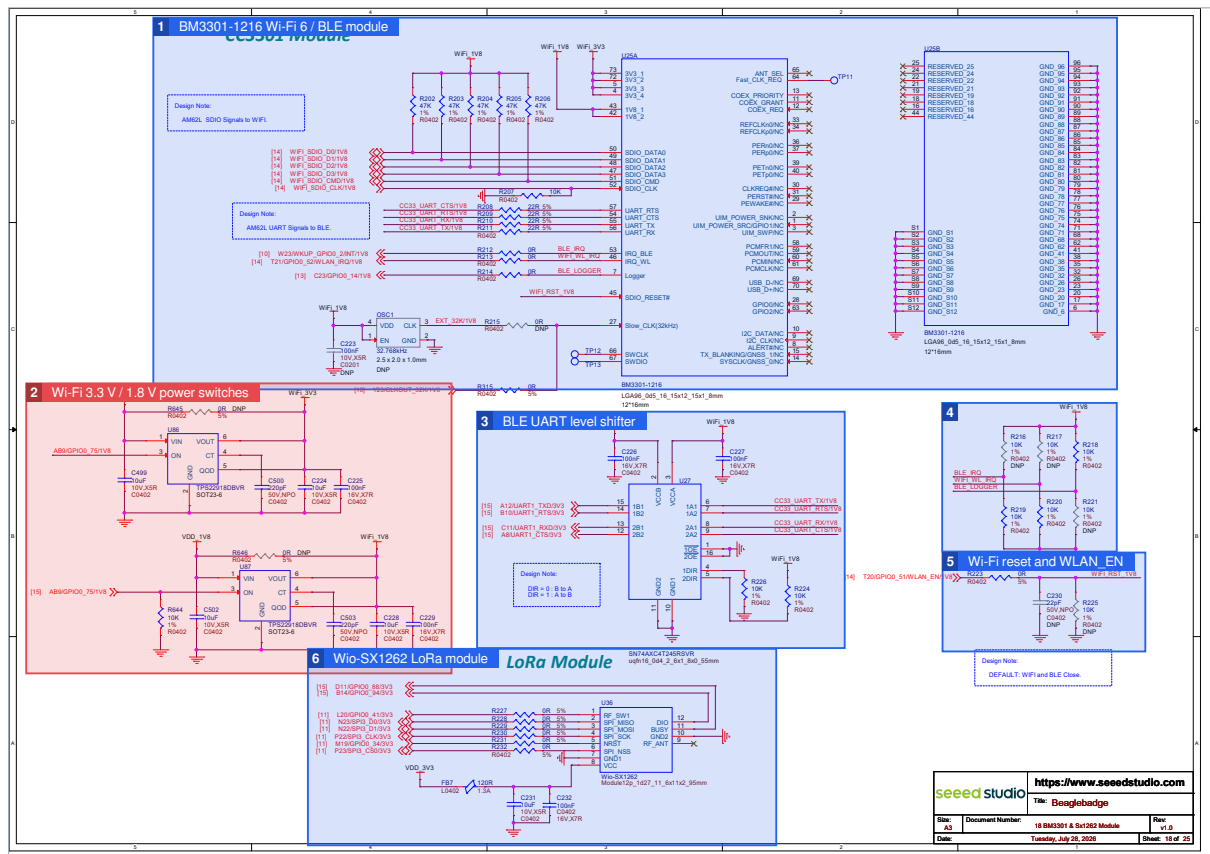
One module covers **862 to 930MHz**, so the same board serves the EU868 and US915 LoRaWAN plans and the other plans in that range. The region is chosen in software, and the antenna must be tuned to match it.

Important

Transmit only on a band that is permitted where you are, and only with an antenna connected to the u.FL connector.

18. BM3301 & SX1262 Module

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Both radios: the BM3301-1216 module on SDIO and UART, and the Wio-SX1262 LoRa module, each with its own power switching and antenna connector.

1 BM3301-1216 Wi-Fi 6 / BLE module WIRELESS U25A U25B OSC1 R202 R206 R207 R215 BeagleMod CC33 page

U25 is the BeagleBoard.org **BeagleMod BM3301-1216** (M.2 1216 LGA) built around the TI CC3301 companion IC: 2.4 GHz **Wi-Fi 6** and **Bluetooth LE 5.4** with an MHF4 antenna connector. Wi-Fi uses the AM62L MMC2 SDIO interface (WIFI_SDIO_*) and BLE uses UART1 with flow control (CC33_UART_*). Interrupts and reset are on WKUP_GPIO0_2, GPIO0_52 and GPIO0_14. OSC1 (32.768 kHz, DNP) is an optional external slow clock. See [Wi-Fi and Bluetooth](#).

2 Wi-Fi 3.3 V / 1.8 V power switches POWER U86 U87 R645 R646 R644 C499 C500 C502 C503 TPS22918 datasheet

U86 and U87 (TPS22918DBVR, 2 A) create the switched WiFi_3V3 and WiFi_1V8 rails from VDD_3V3/VDD_1V8. Both are enabled by AB9/GPIO0_75/1V8 (the *WiFi power switch* added in v1.0), so the radio can be completely powered down. The default state is **off** ("WIFI and BLE close").

3 BLE UART level shifter WIRELESS U27 C226 C227 R226 R224

U27 (SN74AXC4T245) translates the 3.3 V UART1 signals from the SoC to the 1.8 V CC33_UART_* lines of the module. DIR pins are fixed so TX/RTS go A→B and RX/CTS come B→A. OE is tied active.

4 IRQ / logger pull resistors WIRELESS R216 R217 R218 R219 R220 R221

Optional pull-up/pull-down pairs on BLE_IRQ, WIFI_WL_IRQ and BLE_LOGGER (mostly DNP). BLE_LOGGER can be pulled to select the module's debug-log UART mode.

5 Wi-Fi reset and WLAN_EN WIRELESS R223 C230 R225

T20/GPIO0_51/WLAN_EN drives WIFI_RST_1V8 through R223. C230/R225 (DNP) allow adding a power-on reset delay if required.

6 Wio-SX1262 LoRa module WIRELESS U36 R227 R228 R229 R230 R231 R232 FB7 C231 C232 Wio-SX1262 wiki

U36 is the Seeed Studio **Wio-SX1262** (Semtech SX1262) sub-GHz LoRa module with a u.FL antenna connector, connected on SPI3 (SPI3_CS0/CLK/D0/D1) with BUSY/DIO/NRST on GPIO0_41, GPIO0_34 and GPIO0_88/GPIO0_94. FB7 filters its 3.3 V supply. It covers 862-930 MHz and is the radio behind Meshtastic. See [LoRa](#).

3.9 Display

3.9.1 4.2 inch ePaper

The primary display is a 4.2 inch black-and-white electrophoretic (ePaper) module, HINK-E042A162, with a resolution of 400 x 300 pixels and outline dimensions of 97 x 77 x 1.15mm. It attaches through a 24+2 position, 0.5mm pitch top-contact FPC connector (FPC0.5K-DH-24AWB).

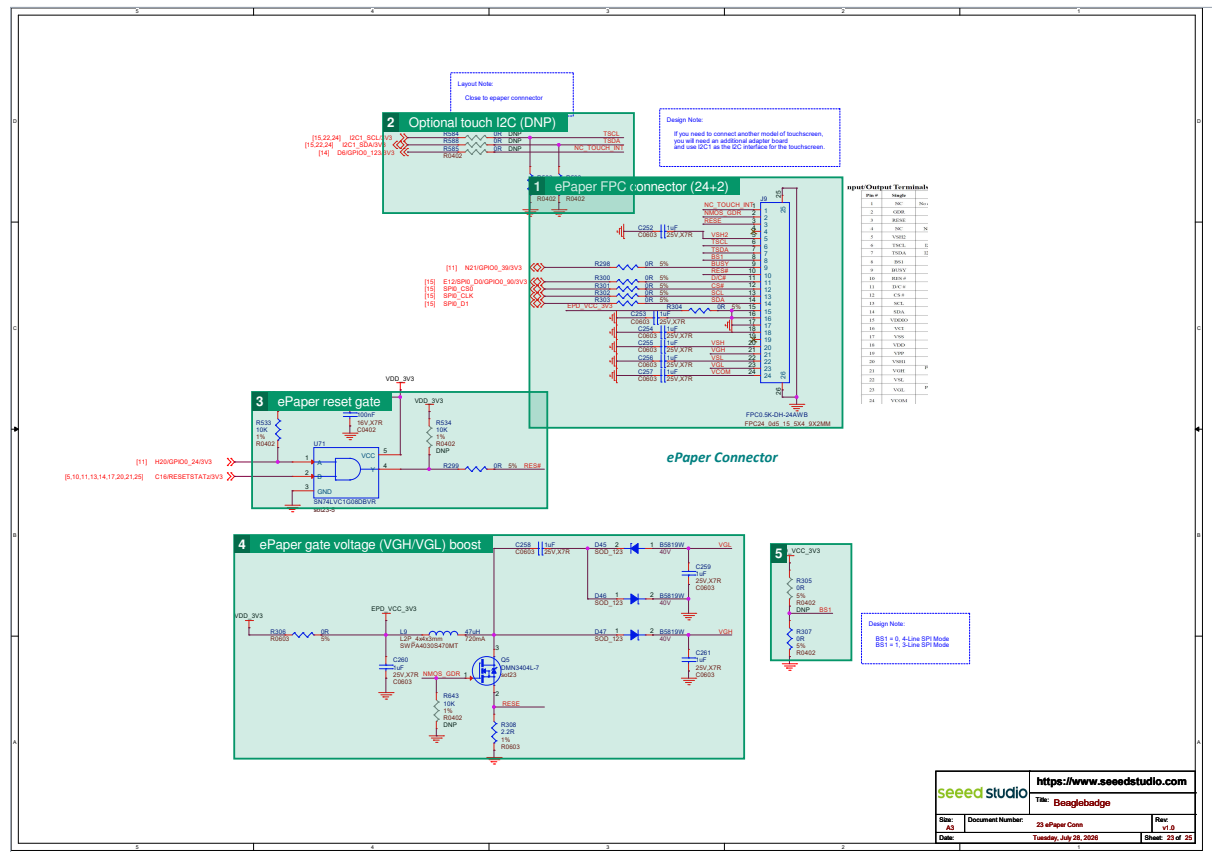
Because the panel is electrophoretic, it draws current only while the image is changing and holds the last image with no power at all, which is what makes multi-day battery operation on a badge practical.

Todo

Confirm the display controller in the HINK-E042A162 panel against its datasheet. The [Zephyr Beagle-Badge board](#) binds a Solomon Systech SSD1681 driver. Once confirmed, add the full and partial refresh times.

23. ePaper Conn

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The 24+2 position FPC connector for the 400 x 300 panel, its SPI interface, the VGH/VGL boost supply and the optional touch I2C lines.

1 ePaper FPC connector (24+2) DISPLAY J9 C252 C253 C254 C255 C256 C257 R298 R300 R304

J9 (FPC0.5K-DH-24AWB, 24+2 position 0.5 mm top-contact) carries the 4-wire SPI (SPIO_CLK, SPIO_D1 as MOSI, SPIO_CS0, D/C# on SPIO_D0/GPIO0_90), RES# and BUSY (GPIO0_39) to the 4.2 in 400 x 300 HINK-E042A162 panel, plus the VSH/VSL/VGH/VGL/VCOM bias caps. See [4.2 inch ePaper](#).

2 Optional touch I2C (DNP) DISPLAY R584 R588 R585 R583 R582

0 Ω links (DNP) that would connect I2C1 and GPIO0_123 to the panel's touch controller pins. For a touch panel of a different model an adapter board is needed. Use I2C1 as the touch interface.

3 ePaper reset gate DISPLAY U71 R533 R534 C381 R299

U71 (SN74LVC1G08) asserts the panel RES# whenever the SoC is in reset or H20/GPIO0_24 is driven low, so the display controller always starts from a known state.

4 ePaper gate voltage (VGH/VGL) boost DISPLAY L9 Q5 D45 D46 D47 C258 C259 C260 C261 R306

R643 R308

The panel controller drives NMOS_GDR to switch Q5 and 47 μH inductor L9, and the diode/capacitor ladder D45-D47 generates the positive and negative gate voltages VGH/VGL from EPD_VCC_3V3. R308 (2.2 Ω) is the current-sense resistor.

5 BS1 SPI mode select DISPLAY R305 R307

BS1 selects the panel interface: R307 fitted (BS1 = 0) gives **4-line SPI** with a separate D/C# pin. R305 fitted (BS1 = 1) selects 3-line SPI.

3.9.2 MIPI DSI

A 22-position, 0.5mm pitch right-angle FPC connector (130-221-220001-W3G) brings out the AM62L32 MIPI DSI interface for attaching a conventional LCD panel.

3.10 Sensors

Table 3.8: On-board sensors

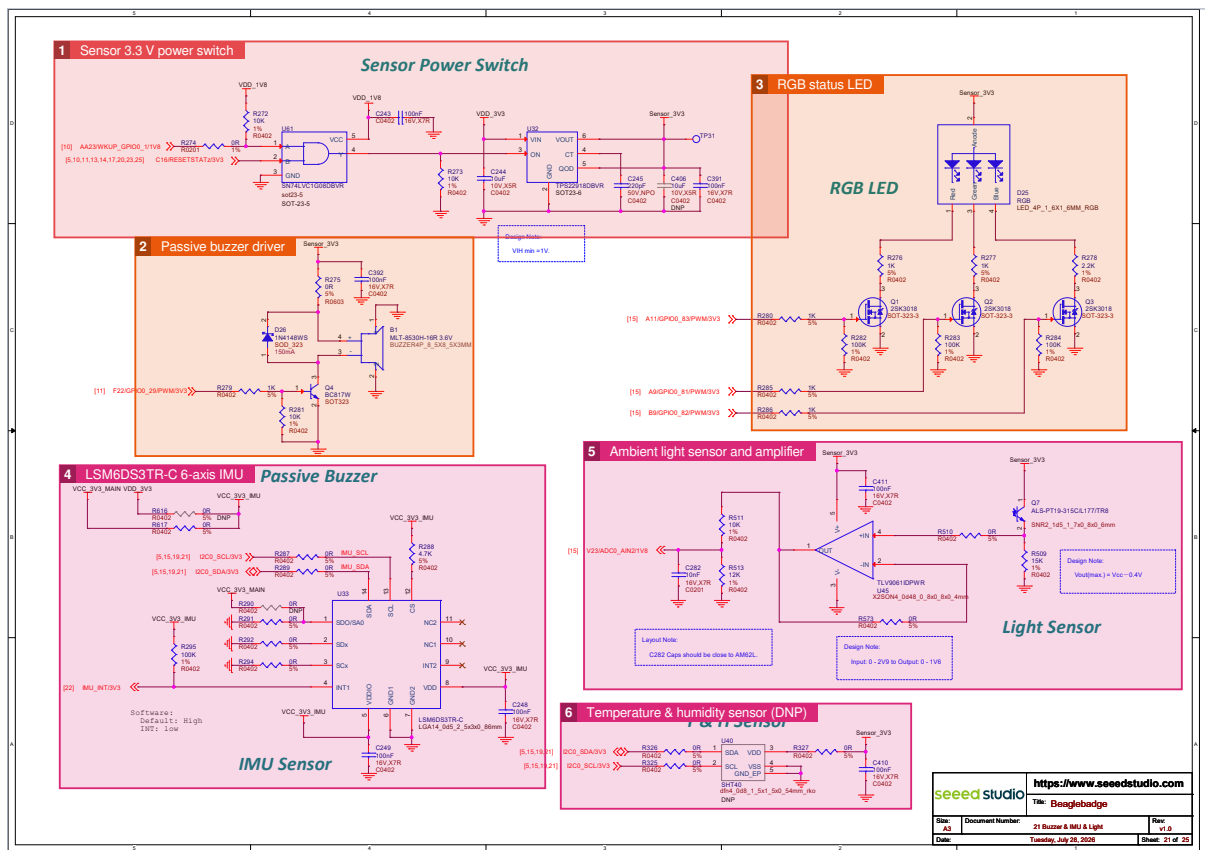
Sensor	Device	Notes
6-axis IMU	ST LSM6DS3TR-C	3-axis accelerometer to +/-16g and 3-axis gyroscope to +/-2000 deg/s, LGA-14
Ambient light	Everlight ALS-PT19-315C	Analog phototransistor, conditioned by a TLV9061 op-amp and read by the AM62L32 ADC
Temperature and humidity	Not populated	Footprint U40 for a Sensirion SHT40

Tip

The temperature and humidity sensor is not populated on v1.0. The U40 footprint takes a Sensirion SHT40 in a 1.5 x 1.5mm DFN package on I2C0, so it can be fitted by hand. The common SHT40-AD1B answers at I2C address 0x44.

21. Buzzer & IMU & Light

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The LSM6DS3TR-C IMU, the ALS-PT19 ambient light sensor with its amplifier, the RGB LED, the passive buzzer, and the unpopulated temperature/humidity footprint.

1 Sensor 3.3 V power switch POWER U61 U32 R272 R274 R273 C244 C245 C406 C391 TP31 TPS22918 datasheet

U32 (TPS22918) produces the switched Sensor_3V3 rail for the IMU, light sensor, RGB LED and 7-segment digits. The AND gate U61 enables it from AA23/WKUP_GPIO0_1 and RESETSTATz so the sensors are off in reset and in low-power modes.

2 Passive buzzer driver USER INTERFACE B1 D26 Q4 R275 R279 R281 C392

B1 (MLT-8530H-16R, passive magnetic buzzer) is driven by NPN transistor Q4 from F22/GPIO0_29/PWM, generate a PWM tone in software. D26 clamps the inductive kick-back. R275 (0 Ω) selects the Sensor_3V3 supply.

3 RGB status LED USER INTERFACE D25 Q1 Q2 Q3 R276 R277 R278 R280 R285 R286

D25 (19-237/R6GHBHC-D02/2T, 1.6 x 1.6 mm common-anode RGB LED) is driven by three N-MOSFETs Q1-Q3 from the PWM-capable GPIO0_83, GPIO0_81 and GPIO0_82. R276/R277 (1 k Ω) and R278 (2.2 k Ω) set the per-colour current.

4 LSM6DS3TR-C 6-axis IMU SENSORS U33 R287 R289 R290 R291 R292 R294 R295 R616 R617 C248 C249 LSM6DS3TR-C datasheet

U33 (ST LSM6DS3TR-C, 3-axis accelerometer ± 16 g + 3-axis gyroscope ± 2000 dps) is on I2C0 (IMU_SCL/IMU_SDA through 0 Ω links). INT1 goes to IMU_INT/3V3 and into the wake-up logic on sheet 22, so motion can wake the badge. v0.5 added R616/R617 to select the IMU supply between VCC_3V3_MAIN and VDD_3V3. See [Sensors](#).

5 Ambient light sensor and amplifier SENSORS U45 Q7 R511 R513 R510 R509 R573 C411 C282 TLV9061 datasheet

Q7 (ALS-PT19-315C, analogue phototransistor) develops a voltage across R509 (15 k Ω) that op-amp U45 (TLV9061) scales (gain ≈ 1.83) into the 0-1.6 V range of V23/ADC0_AIN2. Maximum output is $V_{cc} - 0.4$ V. Keep C282 next to the AM62L ADC pin.

6 Temperature & humidity sensor (DNP) SENSORS U40 R326 R325 R327 C410

Footprint U40 for a Sensirion SHT40 temperature and humidity sensor on I2C0, **not populated** on v1.0. See [Sensors](#).

3.11 User Interface

3.11.1 Buttons and joystick

Table 3.9: Input devices

Device	Qty	Part
5-way joystick	1	BLQ-1502-01-06, 8-pin, 7.5 x 7.5 x 6mm, four directions plus centre press
Push button, 6mm	2	TD-1101SR-C4C-A1R, 6.0 x 6.0 x 5.0mm
Push button, 3x4mm	2	TC-3X4X2.5, 4.6 x 3.2 x 2.5mm, 1.57N actuation force

The four buttons are **BACK** and **SELECT** on the front, either side of the 7-segment digits, **RESET** on the back edge next to the SoC, and a **Power** button added in revision V1.0. SELECT doubles as the boot-source selector at power-on: revision V0.4 merged the boot and select functions onto one button, which is why holding SELECT while applying power boots from microSD (see [Boot from the microSD card](#)).

3.11.2 Indicators and buzzer

Table 3.10: Output devices

Device	Qty	Part
RGB status LED	1	Everlight 19-237/R6GHBHC-D02/2T, 1.6 x 1.6mm
7-segment digits	2	Built from 14 discrete green 0805 LEDs (17-215SYGC/S530-E2/4T)
Indicator LEDs	5	2 x yellow-green and 3 x clear-blue 0603
Passive buzzer	1	MLT-8530H-16R, 2.5-4.5V, 8.5 x 8.5 x 3mm

The two 7-segment digits are driven through a Microchip MCP23S18-E/MJ 16-bit SPI I/O expander with open-drain outputs, which keeps the segment count off the SoC GPIO banks. It sits on SPI1 with chip select SPI1_CS0. The mikroBUS socket uses SPI1_CS1.

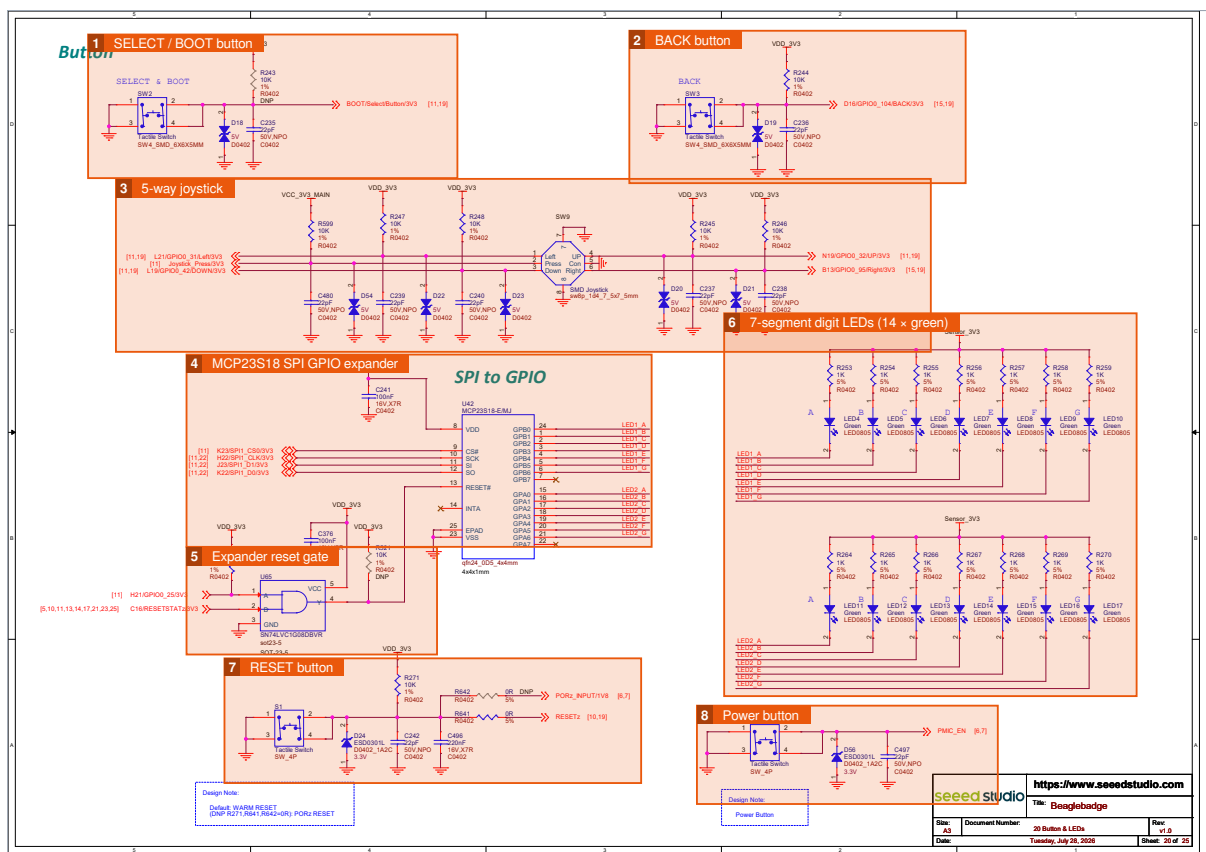
Table 3.11: 7-segment digit mapping

Expander port	Segments
GPB0 to GPB6	Digit 1, segments A to G
GPA0 to GPA6	Digit 2, segments A to G

The expander sinks each segment's cathode, so a segment lights when its bit is driven **low**. The digits are powered from Sensor_3V3, which has to be switched on first.

20. Button & LEDs

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All four push buttons (RESET, power, BACK and the shared SELECT/BOOT button), the 5-way joystick, and the MCP23S18 SPI expander that drives the two 7-segment digits.

1 SELECT / BOOT button USER INTERFACE SW2 R243 D18 C235

SW2 (6 mm tactile) is the front **Select** button. The same net, BOOT/Select/Button/3V3, is also read

by the boot-mode logic on sheet 11: holding it during power-up switches the primary boot from OSPI to **SD card**. D18 is a 5 V ESD diode. R243 (DNP) is an optional pull-up.

2 BACK button USER INTERFACE SW3 R244 D19 C236

SW3 is the front **Back** button on D16/GPIO0_104/BACK, pulled up by R244 with D19 ESD protection and C236 debounce capacitor.

3 5-way joystick USER INTERFACE SW9 R599 R247 R248 R245 R246 D54 D22 D23 D20 D21

SW9 (BLQ-1502-01-06) replaced the four direction buttons in v0.4. Left, Press, Down, Up and Right map to GPIO0_31, Joystick_Press, GPIO0_42, GPIO0_32 and GPIO0_95. Each line has a 10 k Ω pull-up, 22 pF capacitor and ESD diode. The press line can also **wake the system** (sheet 11). See [Buttons and joystick](#).

4 MCP23S18 SPI GPIO expander USER INTERFACE U42 C241 R521 C376 [MCP23S18 datasheet](#)

U42 (MCP23S18-E/MJ, 16-bit SPI I/O expander with open-drain outputs) drives the fourteen 7-segment LEDs from SPI1 (SPI1_CS0/CLK/D0/D1), keeping them off the SoC GPIO banks. GPB0–GPB6 are digit 1 segments A–G and GPA0–GPA6 digit 2. See [Indicators and buzzer](#).

5 Expander reset gate USER INTERFACE U65 R520

U65 (SN74LVC1G08) resets the expander whenever the SoC is in reset (RESETSTATz) or software pulls H21/GPIO0_25 low.

6 7-segment digit LEDs (14 × green) USER INTERFACE LED4 LED10 LED11 LED17 R253 R259 R264 R270

The two 7-segment digits are built from **14 discrete green 0805 LEDs** (17-215SYGC/S530-E2/4T), each with a 1 k Ω resistor to Sensor_3V3. The expander sinks the cathodes, so a segment lights when its bit is driven low.

7 RESET button USER INTERFACE S1 R271 D24 C242 C496 R641 R642

S1 is the **RESET** button on the back edge. By default (R271/R641/R642 = 0 Ω , R642 DNP) it drives RESETz for a *warm* reset. Populating R642 instead routes it to PORz_INPUT for a power-on reset. D24 (ESD0301L) and the 220 nF C496 were added in v1.0 for ESD robustness.

8 Power button USER INTERFACE S2 D56 C497

S2 pulls PMIC_EN to toggle the PMIC and therefore the whole SoC power domain (added in v1.0). This is the fourth push button the BOM lists. It is on the VCC_3V3_MAIN domain so it works while everything else is off.

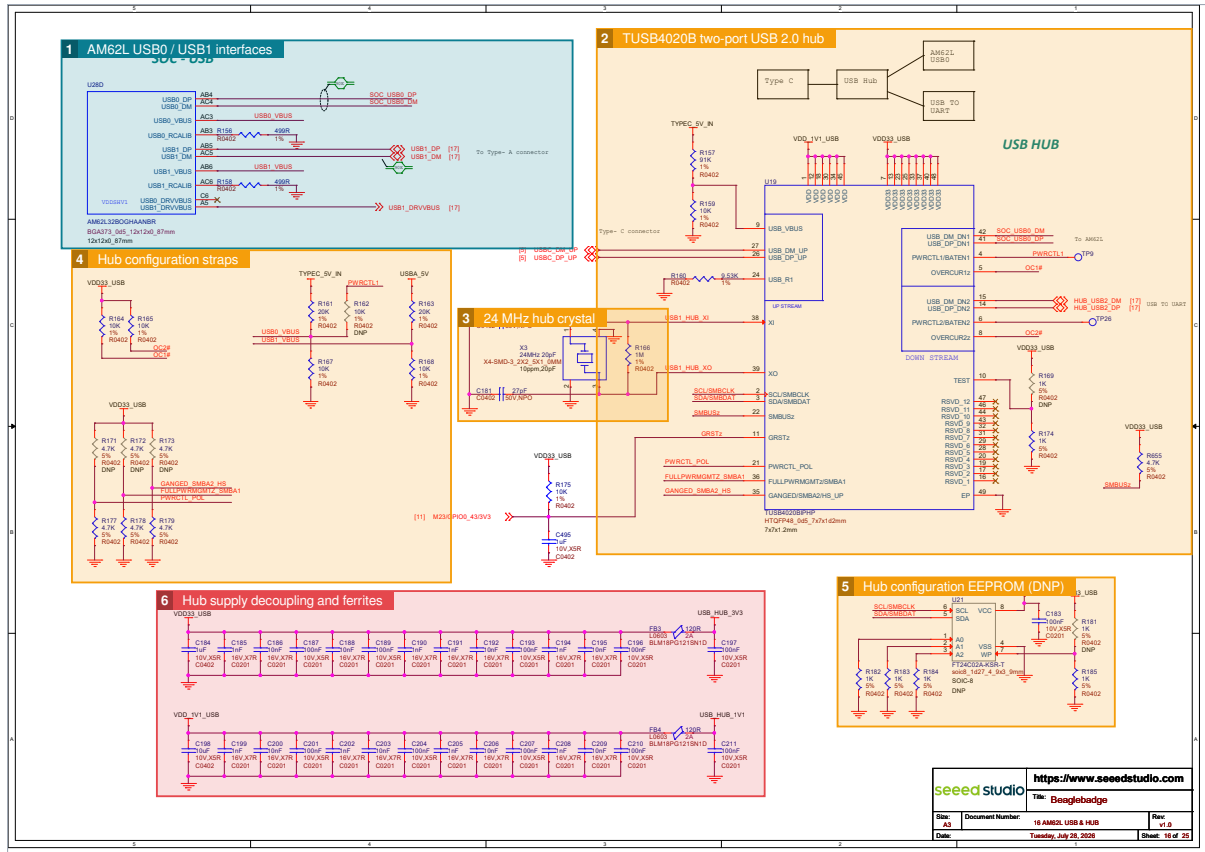
3.12 General connectivity and expansion

3.12.1 USB

Table 3.12: USB interfaces

Port	Description
USB Type-C	UBF31-0171 receptacle used for power input and for the serial debug console.
USB 2.0 Type-A host	U221-041N-4V33-S5 right-angle receptacle for attaching keyboards, storage and other peripherals.

The USB-C data pair goes to the upstream port of a Texas Instruments TUSB4020BIPHR two-port USB 2.0 hub. Downstream port 1 goes to the SoC USB0, so the board appears to a host PC as a USB device, and downstream port 2 goes to the CP2102N console bridge. The hub is powered only while USB-C is connected.



1 AM62L USB0 / USB1 interfaces soc U28D R156 R158

2 TUSB4020B two-port USB 2.0 hub **CONNECTIVITY & EXPANSION** U19 R157 R159 R160 R169 R174 R655 R175

3 24 MHz hub crystal **CONNECTIVITY & EXPANSION** X3 C180 C181 R166

4 **Hub configuration straps** CONNECTIVITY & EXPANSION R161 R162 R163 R167 R168 R171 R172 R173 R177

USB0_VBUS/USB1_VBUS are derived from TYPEC_5V_IN and USBA_5V so the SoC sees VBUS detection.

5 Hub configuration EEPROM (DNP) CONNECTIVITY & EXPANSION U21 C183 R181 R182 R183 R184 R185

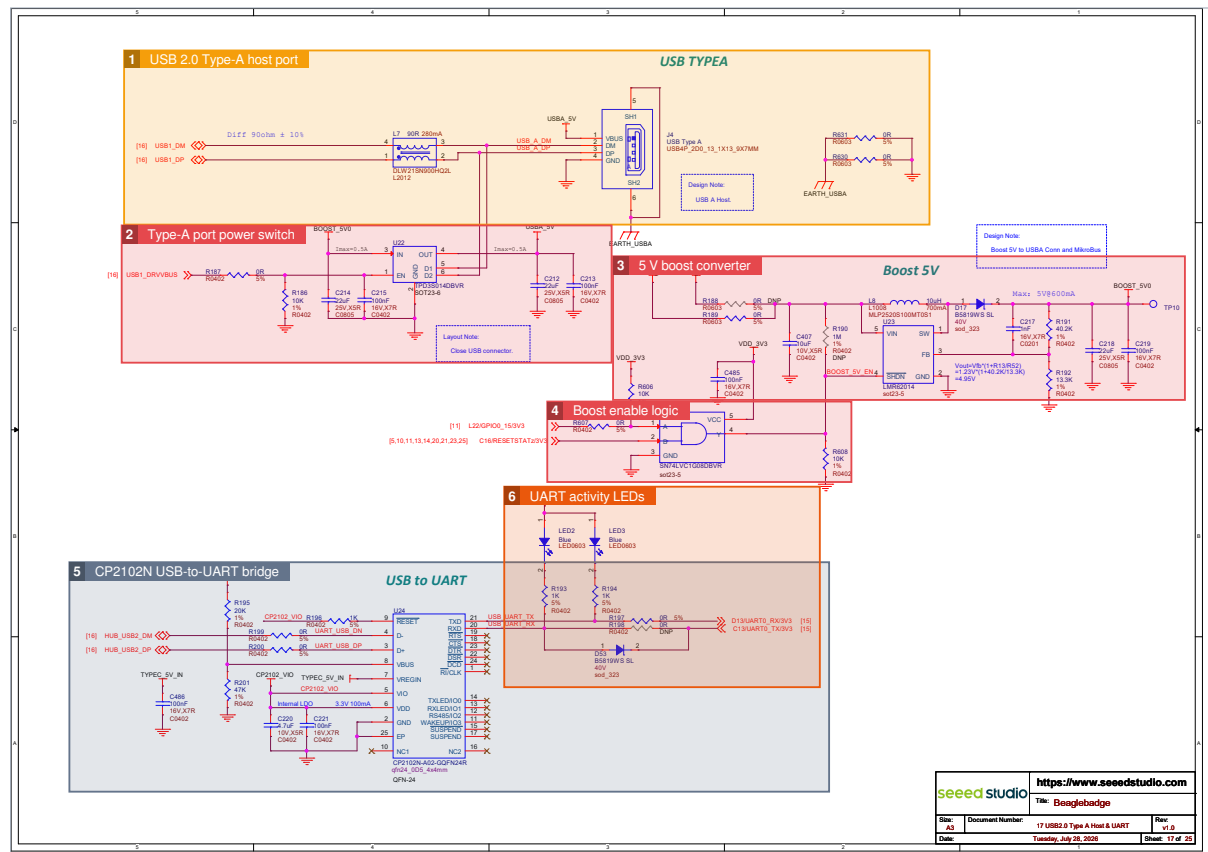
Footprint for an FT24C02A SMBus EEPROM that could hold custom hub descriptors. It is **not populated**. The hub runs from its default configuration.

6 Hub supply decoupling and ferrites POWER FB3 FB4 C184 C197 C198 C211

FB3/FB4 (120 Ω ferrites) isolate VDD33_USB and VDD_1V1_USB from the LDO outputs, with one 1 nF/10 nF/100 nF triplet per hub power pin. Place the 0201 capacitors as close to U19 as possible.

17. USB2.0 Type A Host & UART

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The Type-A host receptacle and its power switch, the 5V boost that supplies it, and the CP2102N bridge that provides the serial console over USB-C.: annotations: usb-a-port, usb-a-power-switch, boost-5v, boost-enable-logate, usb-uart

1 USB 2.0 Type-A host port CONNECTIVITY & EXPANSION J4 L7 R630 R631

J4 (U221-041N-4V33-S5) is a right-angle Type-A receptacle wired directly to AM62L USB1 through the 90 Ω common-mode choke L7. The shield is tied to EARTH_USBA through R630/R631. Use it for keyboards, storage and other peripherals (see [USB](#)).

2 Type-A port power switch POWER U22 R187 R186 C214 C215 C212 C213 TPD3S014 datasheet

U22 (TPD3S014DBVR) switches BOOST_5V0 to USB_A_5V with a 500 mA current limit and integrated ESD protection for the data lines. It is enabled by USB1_DRVVBUS from the SoC, so VBUS is only supplied when the port is in host mode.

3 5 V boost converter POWER U23 L8 D17 C407 R190 R191 R192 C217 C218 C219 [LMR62014 datasheet](#)

U23 (LMR62014XMFE) boosts V_{SYS_OUT} (battery or USB) to BOOST_5V0 for the Type-A port and the mikroBUS 5V pin. R191/R192 (40.2 kΩ / 13.3 kΩ) set $V_{out} = 1.23 \text{ V} \times (1 + 40.2/13.3) \approx \mathbf{4.95 \text{ V}}$, up to 600 mA. R188/R189 (DNP) allow bypassing from VDD_3V3 instead.

4 Boost enable logic POWER U77 R606 R607 R608 C485

The AND gate U77 (SN74LVC1G08) enables the boost converter only when L22/GPIO0_15 is high **and** the SoC is out of reset (RESETSTATz), so the 5 V rail never comes up while the SoC is held in reset.

5 CP2102N USB-to-UART bridge DEBUG U24 R195 R196 R199 R200 R201 C486 C220 C221 [CP2102N datasheet](#)

U24 (CP2102N-A02-GQFN24R) hangs off downstream port 2 of the USB hub and presents the AM62L UART0 console (D13/UART0_RX, C13/UART0_TX) as a virtual COM port on the same USB-C cable that powers the board. V_{REGIN} is fed from TYPEC_5V_IN and the internal 3.3 V LDO powers the part. R201 (47 kΩ) is the V_{BUS} sense divider. See [Serial debug](#).

6 UART activity LEDs USER INTERFACE LED2 LED3 R193 R194 R197 R198 D53

Two blue 0603 LEDs on TXLED/RXLED of the CP2102N blink with console traffic. D53 (B5819WS) keeps the LED supply from back-feeding the bridge.

3.12.2 Ecosystem connectors

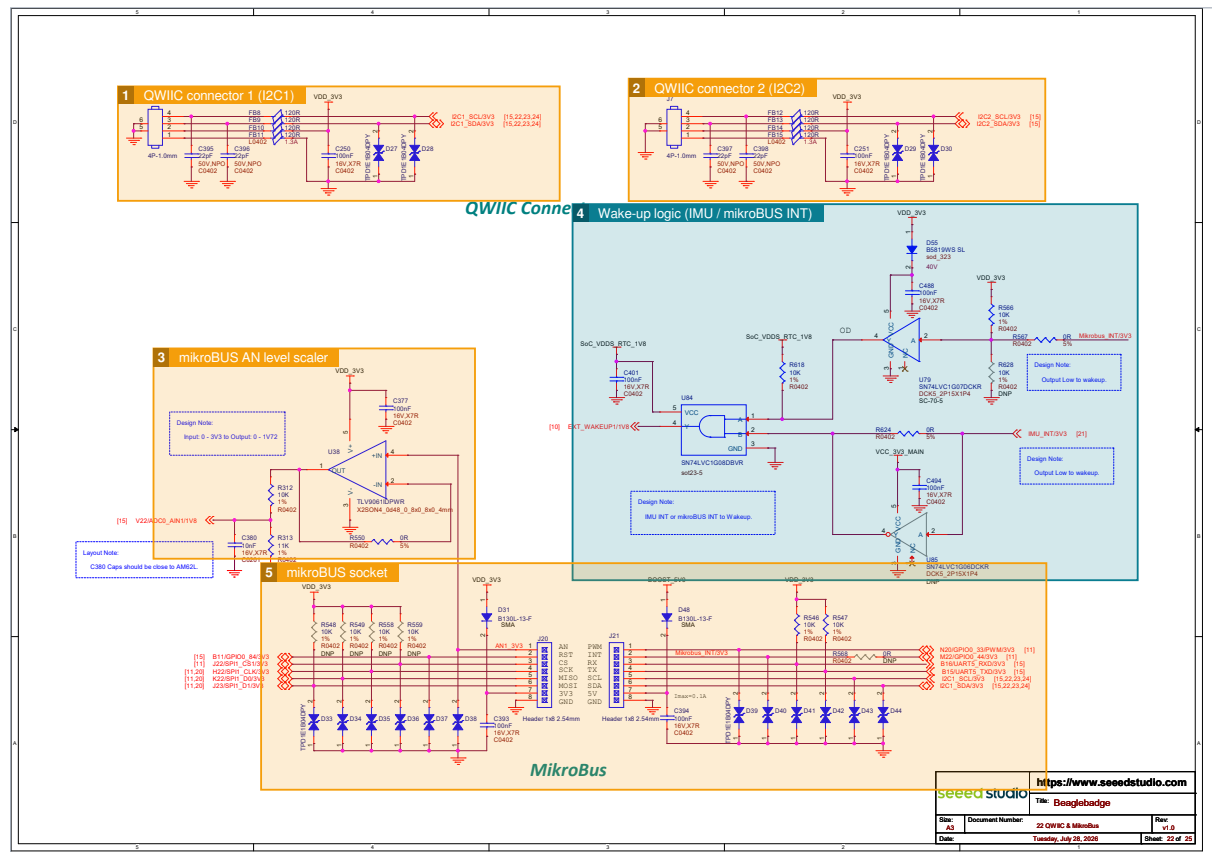
Table 3.13: Expansion connectors

Connector	Qty	Part	Description
QWIIC	2	WY-4539	4-pin, 1.0mm pitch JST-SH style right-angle I2C connectors
Grove	1	PHS-4A	4-pin, 2.0mm pitch right-angle connector
mikroBUS	1	ST-FH-254-0144-1*8P-B x2	A pair of 1x8, 2.54mm pitch vertical female headers

Pinouts for these connectors are covered in [Expansion](#).

22. QWIIC & MikroBus

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Both QWIIC connectors, the mikroBUS socket with its analog input scaler, and the wake-up logic shared between the IMU and the mikroBUS interrupt line.

1 QWIIC connector 1 (I2C1) CONNECTIVITY & EXPANSION J6 FB8 FB9 FB10 FB11 C395 C396 C250 D27 D28

J6 (WY-4539, 4-pin 1.0 mm JST-SH style) exposes I2C1 with VDD_3V3 and GND in the standard **QWIIC / STEMMA QT** pin order. FB8-FB11 and D27/D28 provide EMI filtering and ESD protection. I2C1 is shared with the mikroBUS socket and the DSI connector. See [Ecosystem connectors](#).

2 QWIIC connector 2 (I2C2) CONNECTIVITY & EXPANSION J7 FB12 FB13 FB14 FB15 C397 C398 C251 D29 D30

J7 is the second QWIIC connector, on its own bus I2C2 so that modules with fixed addresses can be used on both connectors at once.

3 mikroBUS AN level scaler CONNECTIVITY & EXPANSION U38 R312 R313 C377 C380 R550

Op-amp U38 (TLV9061) with R312/R313 scales the mikroBUS AN pin (0-3.3 V) down to 0-1.72 V for V22 / ADC0_AIN1, protecting the 1.8 V ADC input.

4 Wake-up logic (IMU / mikroBUS INT) SOC U84 U79 U85 D55 C488 R566 R567 R618 C401 R624 R628 C494

U79 (open-drain buffer) and U84 (AND gate) combine Mikrobus_INT and IMU_INT into EXT_WAKEUP1/1V8 on the SoC wake-up domain: either interrupt going **low** wakes the AM62L from deep sleep. U85 (DNP) is an alternative inverting path.

5 mikroBUS socket CONNECTIVITY & EXPANSION J20 J21 D31 D48 R548 R549 R558 R559 R546 R547 R568

mikroBUS standard

J20/J21 (two 1x8 2.54 mm headers) form the **mikroBUS** socket: AN (scaled to ADC0_AIN1), RST/CS/SCK/MISO/MOSI on SPI1 (shared with the 7-segment expander), PWM on GPIO0_33, INT on

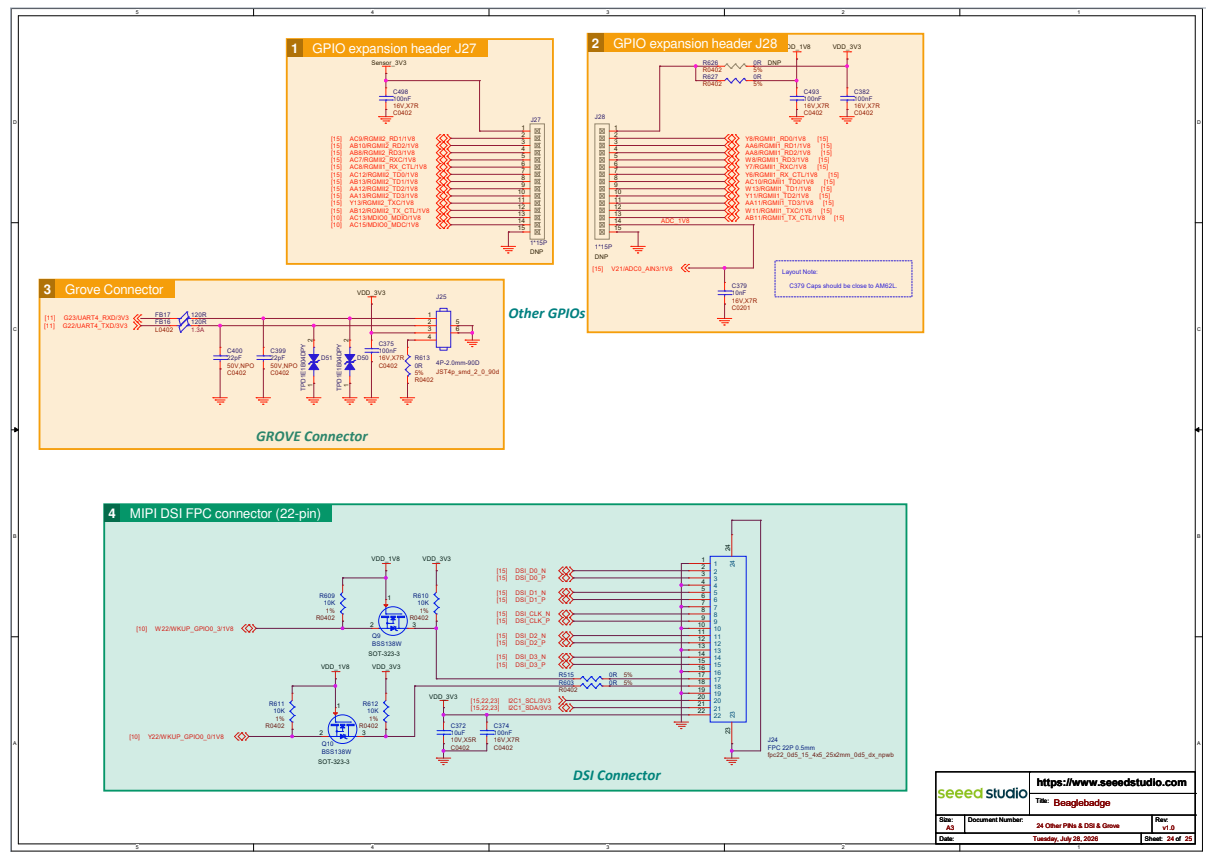
GPIO_44, RX/TX on UART5 and SCL/SDA on I2C1. 5V comes from the boost converter through D48, limited to 0.1 A. Every pin has a TPD1E10B04 ESD diode.

3.12.3 GPIO expansion header

J28 and J27 are two 15-pin headers, not fitted with connectors, that bring out both RGMII ports, the MDIO0 pair, ADC0_AIN3 and the 1.8V and Sensor_3V3 supplies. With no Ethernet PHY on the board, every RGMII pin is available as 1.8V GPIO. The pinout is in [GPIO expansion header](#).

24. Other PINs & DSI & Grove

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Sheet 24 carries three blocks: the two GPIO expansion headers, the Grove connector (wired as an I2C1 port at 3.3V), and the 22-pin FPC connector for a MIPI DSI panel described in [MIPI DSI](#).

1 GPIO expansion header J27 CONNECTIVITY & EXPANSION J27 R609 R610 C372 C493

J27, the right-hand of the two 15-pin headers below the lanyard slot, not fitted with a connector. It carries RGMII2 and the MDIO0 pair as 1.8 V GPIO, with Sensor_3V3 on pin 1 and ground on pin 15. See [GPIO expansion header](#).

2 GPIO expansion header J28 CONNECTIVITY & EXPANSION J28 R611 R612 R613 C374 C375 C498

J28, the left-hand of the two 15-pin headers below the lanyard slot, not fitted with a connector. It carries the 1.8 V supply on pin 1, RGMII1 as 1.8 V GPIO, ADC0_AIN3 on pin 14 and ground on pin 15. See [GPIO expansion header](#).

3 Grove Connector CONNECTIVITY & EXPANSION J25 R626 R627

J25, a 4-pin 2.0 mm right-angle Grove socket wired as an I2C port on I2C1 (I2C1_SCL / I2C1_SDA, 3.3 V), shared with QWIIC connector 1 and the mikroBUS socket. Pin 3 is VDD_3V3 and pin 4 is ground, so Grove

modules that expect a 5 V supply will not work here without a supply adapter. R626 is a DNP option on the bus. See [Grove connector](#).

4 MIPI DSI FPC connector (22-pin) DISPLAY J24 Q9 Q10 D50 D51 C379 C399 C400 R603

J24 (FPC 22P 0.5mm, part 130-221-220001-W3G) carries the four MIPI DSI data lanes and the clock pair from sheet 15 to an LCD panel, with a ground between each pair, I2C1 for a touch controller, and VDD_3V3. Q9 and Q10 (BSS138W) shift WKUP_GPIO0_3 and WKUP_GPIO0_0 from 1.8 V to 3.3 V for pins 17 and 18. The layout note asks for C379 to be placed close to the SoC. See [FPC connectors](#).

3.13 Debug Ports

3.13.1 Serial debug

A Silicon Labs CP2102N-A02-GQFN24R USB-to-UART bridge is fitted on-board and shares the USB Type-C connector, so a single cable carries power and the console with no debug probe required. The console is presented on the SoC `main_uart0` interface.

Port settings and host device names are in [Serial console](#).

3.13.2 JTAG

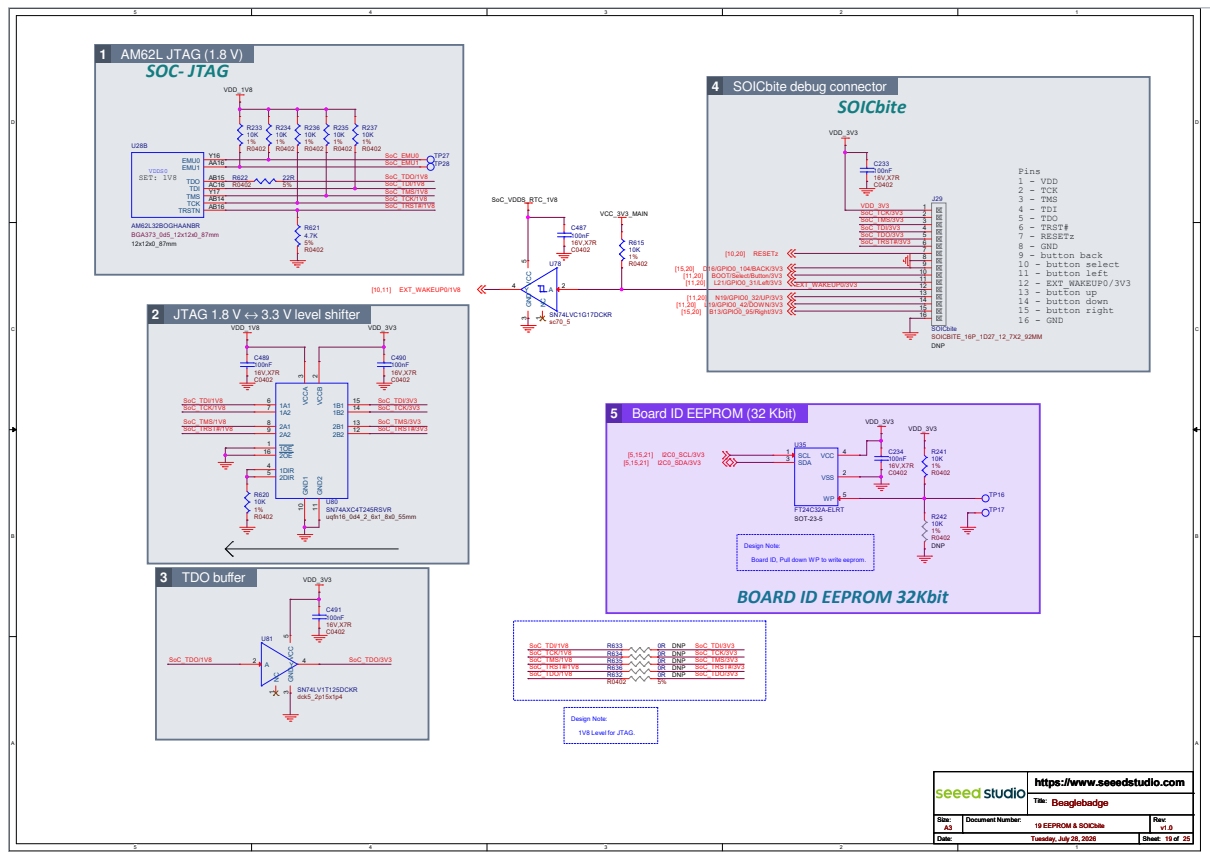
The board exposes JTAG on an edge SOICbite connector, which allows a standard SOIC test clip to be used for hardware-level debugging without fitting a dedicated header.

Todo

Add the J29 pinout table from [schematic sheet 19](#).

19. EEPROM & SOICbite

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The SoC JTAG pins, the 1.8V to 3.3V buffer added in revision V0.7, the SOIC16 SOICbite debug footprint and the 32Kbit board-identity EEPROM.

1 AM62L JTAG (1.8 V) DEBUG U28B R233 R234 R235 R236 R237 R622 R621

The AM62L TDO/TDI/TMS/TCK/TRSTn pins live in the 1.8 V VDDSD0 domain with 10 kΩ pull-ups (R233-R237). EMU0/EMU1 are brought to test points TP27/TP28. See [JTAG](#).

2 JTAG 1.8 V ↔ 3.3 V level shifter DEBUG U80 C489 C490 R620

U80 (SN74AXC4T245) translates TDI, TCK, TMS and TRST# from the 3.3 V SOICbite side to the 1.8 V SoC side (v0.7 change: *JTAG signals to 3.3 V through a buffer*). R633-R636 (DNP, bottom of sheet) can bypass the shifter.

3 TDO buffer DEBUG U81 C491

U81 (SN74LV1T125) buffers SoC_TDO/1V8 out to 3.3 V for the debug probe.

4 SOICbite debug connector DEBUG J29 C233 U78 C487 R615 SOICbite project

J29 is a **SOICbite** footprint: a SOIC-16 land pattern that accepts a standard test clip instead of a dedicated header. Pins 1-8 carry JTAG and RESETz, pins 9-15 bring out the Back/Select/joystick button lines and EXT_WAKEUP0, pin 16 is GND (the full pin list is printed on the sheet). U78 buffers EXT_WAKEUP0 into the 1.8 V wake-up domain. See [JTAG](#).

5 Board ID EEPROM (32 Kbit) MEMORY & STORAGE U35 C234 R241 R242 TP16 TP17

U35 (FT24C32A-ELRT, 32 Kbit I2C EEPROM, SOT23-5) on I2C0 holds the board identity written at manufacturing, following the BeagleBoard.org convention. WP is pulled up by R241. **pull "TP16" low to write the EEPROM.** See [Storage](#).

3.14 Mechanical specifications

3.14.1 Dimensions and weight

Table 3.14: Dimensions and weight

Parameter	Value
Board size	110 x 91 mm
PCB layers	6 layers
PCB thickness	1.6 mm
PCB colour	Black
ePaper module	97 x 77 x 1.15 mm
Mounting	4 x M2 bronze standoffs (SMTSO2015CTJ-UL, 5.56 x 1.5mm)
Gross weight	See Known gaps and open questions
Net weight	See Known gaps and open questions

The 6-layer stackup is, from top to bottom: L1_TOP, L2_GND1, L3_SIG1, L4_SIG2, L5_PWR, L6_BOTTOM.

Todo

Add a dimensioned drawing and the top and bottom silkscreen images, exported from the board files in the [BeagleBadge repository](#), and the measured board weight.

Chapter 4

Expansion

BeagleBadge does not use the BeagleBone cape headers. Instead it expands through three types of industry-standard ecosystem connectors, so that off-the-shelf modules can be attached without designing a custom board. BeagleBadge has two QWIIC connectors, one Grove connector and one mikroBUS socket. A row of 1.8V GPIO and ADC pads along the top edge covers everything else, and two FPC connectors carry the ePaper panel and a MIPI DSI display.

Note

The pin order of each connector is fixed by its ecosystem. What varies between boards is which SoC peripheral lands on each pin. Both are given below, read from [the schematic](#). Anything still unconfirmed is marked.

4.1 Pinout diagrams

Todo

Add pinout diagrams for the QWIIC, Grove, mikroBUS and GPIO expansion headers in the style of the bbai64-expansion diagrams, marking pin 1 of each.

4.2 QWIIC connectors

BeagleBadge has **two** QWIIC connectors (WY-4539), 4-pin 1.0mm pitch JST-SH style, right-angle. QWIIC is a 3.3V I2C-only ecosystem, which means devices can be daisy-chained and hot-plugged without soldering.

Table 4.1: QWIIC connector pinout (standard)

Pin	Signal	Cable colour	Notes
1	GND	Black	Ground
2	3.3V	Red	Supply, VDD_3V3
3	SDA	Blue	I2C data
4	SCL	Yellow	I2C clock

The two connectors are on **separate buses**: QWIIC 1 (J6) is on I2C1, shared with the mikroBUS socket, the Grove connector and the ePaper touch option. QWIIC 2 (J7) is on I2C2 by itself. That means a module with a fixed I2C address can be used on both connectors at the same time. Both are filtered with ferrite beads and ESD diodes.

Both buses are pulled up to VDD_3V3 with 4.7kΩ resistors beside the SoC, on [schematic sheet 15](#), so a module does not need pull-ups of its own. Many QWIIC modules fit them anyway. With several such modules on one bus, disable the extra pull-ups, usually with a solder jumper on the module.

The 3.3V pin is VDD_3V3 through a ferrite bead rated 1.3A, with no current limit or fuse of its own. The same rail supplies the SoC I/O, the ePaper panel and the other expansion connectors, so the practical budget is set by the battery. See [Powering expansion hardware](#).

4.3 Grove connector

BeagleBadge has **one** Grove connector (PHS-4A), 4-pin 2.0mm pitch, right-angle.

Table 4.2: Grove connector pinout (standard I2C variant)

Pin	Signal	Cable colour	Notes
1	SCL	Yellow	I2C clock on an I2C Grove port
2	SDA	White	I2C data on an I2C Grove port
3	VCC	Red	Supply
4	GND	Black	Ground

Important

This is an **I2C** Grove port at **3.3V**, on I2C1. Grove modules that expect a 5V supply, or that use the UART, analog or digital Grove variants, will not work here without an adapter.

4.4 mikroBUS socket

BeagleBadge has **one** mikroBUS socket, built from a pair of 1x8, 2.54mm pitch vertical female headers (ST-FH-254-0144-1*8P-B). mikroBUS is a MikroElektronika standard that gives access to SPI, I2C, UART, PWM, analog and interrupt lines from a single socket, and there are well over a thousand Click boards available for it.

Table 4.3: mikroBUS socket pinout

Pin	Signal	BeagleBadge function	Pin	Signal	BeagleBadge function
1	AN	ADC0_AIN1, scaled	16	PWM	GPIO0_33
2	RST	SPI1 group	15	INT	GPIO0_44
3	CS	SPI1 chip select	14	RX	UART5_RXD
4	SCK	SPI1 clock	13	TX	UART5_TXD
5	MISO	SPI1 data out	12	SCL	I2C1_SCL
6	MOSI	SPI1 data in	11	SDA	I2C1_SDA
7	+3.3V	VDD_3V3	10	+5V	Boost converter, 0.1A max
8	GND	Ground	9	GND	Ground

SPI1 is shared with the 7-segment display expander, and I2C1 with QWIIC connector 1 and the Grove connector. Every pin carries an ESD diode.

Warning

The 5V pin is fed from the on-board boost converter through a diode and is limited to **0.1A**. Click boards that draw more than that from 5V will not work reliably on battery power.

4.5 GPIO expansion header

Two 15-pin headers, J28 on the left and J27 on the right, sit side by side across the front of the board just below the lanyard slot. No connector is fitted. Instead of sitting in a straight line, the plated holes zig-zag, they alternate slightly above and below the centre line of a standard header footprint. A pin header pushed into the row is gripped by the staggered holes, so it makes contact without soldering.

The silkscreen prints the AM62L32 ball name beside each hole rather than a GPIO number. BeagleBadge fits no Ethernet PHY, so both RGMII ports and the MDIO0 pair are free for use as general-purpose I/O. Pins are numbered left to right as you look at the front of the board: 1-15 on J28 and 16-30 on J27.

Warning

Signal pins are **1.8V**. Connecting 3.3V or 5V logic directly risks damaging the SoC, so use a level translator.

J28 (Pin 1-15)

Table 4.4: J28, left header

Pin	Silkscreen	Signal
1	1V8	1.8V supply
2	Y8	RGMII1_RD0
3	AA6	RGMII1_RD1
4	AA8	RGMII1_RD2
5	W8	RGMII1_RD3
6	Y7	RGMII1_RXC
7	Y6	RGMII1_RX_CTL
8	AC10	RGMII1_TD0
9	W13	RGMII1_TD1
10	Y11	RGMII1_TD2
11	AA11	RGMII1_TD3
12	W11	RGMII1_TXC
13	AB11	RGMII1_TX_CTL
14	V21	ADC0_AIN3, analog input, 0 to 1.8V
15	GND	Ground

J27 (Pin 16-30)

The schematic numbers J27's own pins 1-15, so pin 16 here is J27 pin 1.

Pin 16 carries `Sensor_3V3`, the switched 3.3V rail that also feeds the IMU, light sensor, RGB LED and 7-segment digits. It is on only while `WKUP_GPIO0_1` enables it, so switch it on in software before powering anything from this pin.

Note

On schematic sheets 15 and 24 the net label for ball AC8 reads `RGMII1_RX_CTL`, but the SoC symbol names that ball `RGMII2_RX_CTL`, which is what the pinout above shows.

Todo

Add the Linux GPIO chip and line number for each signal pin, read back from a running board with `gpioinfo` (`libgpiod`), so the header can be driven without working back from ball names. The ball-to-signal mapping is on [schematic sheet 15](#).

4.6 FPC connectors

Table 4.5: FPC connectors

Connector	Positions	Part	Purpose
ePaper	24+2, 0.5mm	FPC0.5K-DH-24AWB	4.2 inch 400x300 black-and-white ePaper panel, top contact
MIPI DSI	22, 0.5mm	130-221-220001-W3G	LCD panel, right-angle bottom contact

J9 ePaper (24+2 pin)

Table 4.6: J9 ePaper connector pinout

Pin	Signal	BeagleBadge connection
1	NC	NC_TOUCH_INT, touch interrupt option, link to GPIO0_123 not fitted
2	GDR	NMOS_GDR, gate drive for the VGH/VGL boost
3	RESE	Boost current sense
4	NC	Not connected
5	VSH2	Decoupled to ground
6	TSCL	Touch I2C clock, link to I2C1_SCL not fitted
7	TSDA	Touch I2C data, link to I2C1_SDA not fitted
8	BS1	Interface select, tied for 4-line SPI
9	BUSY	GPIO0_39
10	RES#	Panel reset, from GPIO0_24 gated by RESETSTATz
11	D/C#	SPI0_D0, used as the data/command GPIO GPIO0_90
12	CS#	SPI0_CS0
13	SCL	SPI0_CLK
14	SDA	SPI0_D1, data to the panel
15	VDDIO	EPD_VCC_3V3
16	VCI	EPD_VCC_3V3
17	VSS	Ground
18	VDD	Decoupled to ground
19	VPP	Not connected
20	VSH1	Decoupled to ground
21	VGH	Gate high voltage from the on-board boost
22	VSL	Decoupled to ground
23	VGL	Gate low voltage from the on-board boost
24	VCOM	Decoupled to ground
25, 26	Mounting	Ground

The signal names are the panel's own.

J24 MIPI DSI (22 pin)

Table 4.7: J24 MIPI DSI connector pinout

Pin	Signal	BeagleBadge connection
1	GND	Ground
2	D0_N	DSI_D0_N
3	D0_P	DSI_D0_P
4	GND	Ground
5	D1_N	DSI_D1_N
6	D1_P	DSI_D1_P
7	GND	Ground
8	CLK_N	DSI_CLK_N
9	CLK_P	DSI_CLK_P
10	GND	Ground
11	D2_N	DSI_D2_N
12	D2_P	DSI_D2_P
13	GND	Ground
14	D3_N	DSI_D3_N
15	D3_P	DSI_D3_P
16	GND	Ground
17	GPIO	WKUP_GPIO0_3, shifted from 1.8V to 3.3V
18	GPIO	WKUP_GPIO0_0, shifted from 1.8V to 3.3V
19	GND	Ground
20	SCL	I2C1_SCL
21	SDA	I2C1_SDA
22	3.3V	VDD_3V3
23, 24	Mounting	Ground

All four DSI data lanes are routed, so the connector supports the SoC's full DSI output of up to 1920x1080 at 60fps. Pins 17 and 18 go through BSS138 level shifters with 10kΩ pull-ups on both sides, and can be used for panel reset or backlight enable.

Todo

List LCD panels that have been tested on J24, with the device tree overlay each one needs.

4.7 Antenna connectors

Table 4.8: Antenna connectors

Connector	Type	Radio
Wi-Fi / BLE	IPEX Gen 4 (MHF4)	BeagleMod BM3301-1216 module (TI CC3301)
LoRa	u.FL	Wio-SX1262 module

Todo

List antennas known to work on the IPEX Gen 4 (Wi-Fi and BLE) and u.FL (LoRa) connectors. The BM3301-1216 module is certified with specific antennas. See the [BeagleMod CC33 page](#).

4.8 Powering expansion hardware

The QWIIC, Grove and mikroBUS 3.3V pins are on VDD_3V3, which is ON whenever the board is ON and has no separate switch. The mikroBUS 5V pin comes from the boost converter and is limited to 0.1A. GPIO expansion header pin 16 is Sensor_3V3, which software must switch on. See [Rails, converters and load switches](#).

 Warning

On battery, every milliamp drawn by expansion hardware comes out of a single BL-5C cell. Budget carefully before attaching several modules at once.

Chapter 5

Demos and Tutorials

The fastest way to see what BeagleBadge can do is to write the demo image to a microSD card and boot from it. Nothing on the board is overwritten, so you can return to whatever was installed before by removing the card.

5.1 Embedded World 2026 demo image

An Armbian image built for Embedded World 2026 is published on the BeagleBoard.org distros page. It is a minimal Debian `trixie` userland with the BeagleBadge device tree and ePaper support already in place.

Image	Armbian BeagleBadge demo for EW 2026
Version	Armbian 26.02.0-trunk, Debian <code>trixie</code> , kernel 6.12.57, minimal
File	Armbian-EW_root_beagle_26.02.0-trunk_Beaglebadge_trixie_vendor-edge_6.12.57_minimal.img.xz.zip
SHA256	6b1dbb155a22e2ed72dd868996fabfbf7aa69ae0432dc43f86214ca7b34628f6

5.1.1 Download and verify

Download the image from the distros page above, then check it against the published checksum before writing it:

Linux

```
sha256sum Armbian-EW_root_beagle_*.img.xz.zip
```

macOS

```
shasum -a 256 Armbian-EW_root_beagle_*.img.xz.zip
```

Windows

```
certutil -hashfile Armbian-EW_root_beagle_*.img.xz.zip SHA256
```

The download is a `.zip` wrapping an `.img.xz`. Extract the `.zip` first so that you are left with a single `.img.xz` file, which both of the writers below accept directly, there is no need to decompress it any further.

5.1.2 Write the image to a microSD card

You need a microSD card of 8GB or larger and a card reader.

Tip

If you are using a Linux system, you can write the image from the command line with `xz-cat Armbian-EW_root_beagle_*.img.xz | sudo dd of=/dev/sdX bs=4M conv=fsync` where `/dev/sdX` is the device name of your card. Check it carefully before running the command, as it will overwrite whatever is on that device.

Important

Writing the image to the card will erase whatever is on it. Make sure you have selected the correct device before proceeding.

bb-imager

Download and install [bb-imager](#) for your operating system, then:

1. Click **CHOOSE DEVICE**. If BeagleBadge is not in the list, pick **No filtering** so that every image type is offered.
2. Click **CHOOSE OS**, scroll to the bottom and select **Use custom image**, then browse to the `.img.xz` you extracted.
3. Click **CHOOSE STORAGE** and select your microSD card. Check the device size carefully before continuing.
4. Click **NEXT** and confirm. Skip the customisation settings. The demo image supplies its own configuration.
5. Wait for writing and verification to finish, then eject the card.

Tip

The same walkthrough with screenshots, for a board that is listed by name, is in the BeagleY-AI quick start. The only step that differs for BeagleBadge is choosing a custom image instead of a named OS.

balenaEtcher

Download and install [balenaEtcher](#), then:

1. Click **Flash** from **file** and select the `.img.xz`.
2. Click **Select target** and choose your microSD card.
3. Click **Flash** and wait for the write and validation to complete.

Etcher decompresses the image as it writes, so the `.img.xz` does not need to be unpacked first.

5.1.3 Boot from the microSD card

1. Insert the microSD card into the socket on the back of the board.
2. **Hold down SELECT** on the front.

3. While still holding SELECT, switch the board ON by simply connecting a USB Type-C cable, or press the Power button if it is running from a battery.
4. Release SELECT after a couple of seconds. The boot device is chosen the moment power is applied.

To boot from the card again after a RESET, switch the board OFF and ON with SELECT held. RESET keeps the current boot device. See [Boot Modes](#).

If the board does not start from the card, it has moved on to its backup boot device, USB DFU, and is waiting on the USB connection. Check that the image was written to the whole card rather than to a partition on it, that the card is fully seated, and that SELECT was held until power was applied.

5.1.4 Watching it boot

If you want to see what is happening rather than guess, attach a serial console over the same USB-C cable that powers the board and watch the boot log. Settings are in [Serial debug](#).

Todo

Add a photograph of the EW 2026 demo on the ePaper panel, and describe what it shows at first boot and what the joystick, BACK and SELECT do within it.

5.2 Tutorials

The tutorials below are still to be written. Each one is a page under `boards/beaglebadge/demos-and-tutorials/`, added to a toctree here in the same way as `bbai64-demos-and-tutorials`.

5.2.1 Display

Todo

Draw to the ePaper panel from Linux.

Todo

Build an interface for the ePaper panel with LVGL.

Todo

Drive the ePaper panel from MicroPython.

Todo

Compare full and partial refresh of the ePaper panel, and what each costs in battery life.

5.2.2 Sensors

Todo

Read the IMU, including tap and orientation detection. See [Sensors](#).

Todo

Read the ambient light sensor through ADC0_AIN2.

Todo

Rotate the display to match the orientation reported by the IMU.

5.2.3 Controls and indicators

Todo

Read the joystick and buttons as Linux input events. See [Buttons and joystick](#).

Todo

Drive the RGB status LED.

Todo

Drive the 7-segment digits through the MCP23S18 expander, using the segment mapping in [Indicators and buzzer](#).

Todo

Play tones on the passive buzzer.

5.2.4 Wireless

Todo

Join a Wi-Fi network, including switching the radio's power on. See [Wi-Fi and Bluetooth](#).

Todo

Use Bluetooth Low Energy.

 Todo

Send and receive LoRa messages. See [LoRa](#).

 Todo

Run Meshtastic for off-grid messaging.

 Todo

Set up the ActivityPub integration.

5.2.5 Expansion

 Todo

Add a QWIIC sensor. See [QWIIC connectors](#).

 Todo

Add a Grove module. See [Grove connector](#).

 Todo

Use a mikroBUS Click board. See [mikroBUS socket](#).

5.2.6 Power

 Todo

Read state of charge from the BQ27220 fuel gauge. See [Battery charging and power path](#).

 Todo

Measure battery life and extend it with the SoC low power modes. See [Low power modes](#).

5.3 Zephyr

BeagleBadge has an upstream Zephyr board port, with the board target `beaglebadge/am6213/a53`. Building and running a Zephyr application is covered in [Running Zephyr](#).

Chapter 6

Additional Support Information

All support for this design is through BeagleBoard.org community at [BeagleBoard.org forum](https://beagleboard.org/forum).

6.1 Certifications and export control

6.1.1 Export designations

- HS: 8471504090
- US HS: 8517180050
- EU HS: 8471707000
- Country of origin: China

Todo

Add the FCC, CE and UKCA status of the assembled board.

6.2 Hardware Design

All BeagleBadge hardware design files are published in the [BeagleBadge repository](#) under the `design/` folder.

Table 6.1: Design files

File	Contents
BeagleBadge_V1.0_SCH_260728.pdf	Schematic, revision V1.0
BeagleBadge_V1.0_260826.brd	Board layout
BeagleBadge_BOM.csv	Bill of materials
design/gerber/	Gerber artwork and drill files for the 6-layer stackup

Design files are licensed under the [Creative Commons Attribution-ShareAlike 4.0 International License](#). The upstream documentation is licensed under the MIT License.

6.3 Software Updates

The current demo image and how to write it are in [Embedded World 2026 demo image](#). Updating an installed image is covered in [Updating the installed software](#).

6.4 RMA Support

If you feel your board is defective or has issues, request a Return Merchandise Authorization (RMA) by filling out the form at <http://beagleboard.org/support/rma>. You will need the serial number and revision of the board.

Todo

Add a photograph showing where the serial number and revision are printed on the board.

6.5 Getting Help

If you need up to date troubleshooting techniques, post your questions on the [BeagleBoard.org forum](https://beagleboard.org/forum).

Issues with the hardware design itself can be raised on the [BeagleBadge issue tracker](#).

6.6 Known gaps and open questions

These points are not yet documented or not yet confirmed. Each links to the section where it will be filled in.

Table 6.2: Open questions

Topic	Gap	Where it appears
Weight	Not yet measured.	Dimensions and weight
GPIO numbers	Linux GPIO chip and line numbers for the expansion header pins.	GPIO expansion header

6.7 Change History

This section describes the change history of this document and board. Document changes are not always a result of a board change. A board change will always result in a document change.

6.7.1 Document Change History

Table 6.3: Document change history

Rev	Changes	Date	By
0.0.1	Initial BeagleBadge documentation	August 2026	Deepak Khatri
0.0.2	All 25 schematic sheets embedded and annotated, board revision history added from schematic sheet 1	September 2026	Deepak Khatri

6.7.2 Board Changes

The authoritative board revision history is printed on sheet 1 of the schematic, which is reproduced at [Table of contents and revision history](#). It is summarised below. Also check the [issues list](#) in the [BeagleBadge repository](#).

Table 6.4: Board revision history

Rev	Date	Main modifications
Rev A	14 October 2025	Initial release.
V0.3	20 October 2025	Capacitor withstand voltage raised to 2x or higher. AND gate schematic symbol corrected. Switch control added to the power monitoring ADC. RTC_PG and PMIC circuit modified to reset the AM62L. Output capacitor of TPS22965DSGR marked DNI. eMMC circuit added . Wake-up signals WAKEUP0/WAKEUP1 corrected. Tag-Connect changed to a SOIC16 bite . Button GPIOs moved to 3.3V I/O because they connect to the SOICbite. I2C signals left unpopulated for touchscreen compatibility.
V0.4	24 October 2025	U9 replaced with 0R resistors to switch low power mode. Boot and Select functions merged onto one button . Up/Down/Left/Right buttons replaced with a joystick . SPI1 used to connect U42 (SPI to GPIO) and mikroBUS. Network identification descriptions corrected and extended. Some GPIO allocation adjusted.
V0.5	28 October 2025	Power supply selection added for the IMU. U62 circuit modified to prevent its input floating. EXT_WAKEUP0 added to pin 12 of J29 (SOICbite).
V0.6	29 October 2025	M23/GPIO0_43/3V3 used to reset the USB hub. F22/GPIO0_29/PWM/3V3 used to drive the buzzer. RGB LED changed to a smaller package.
V0.7	5 November 2025	Sheet 8: VDDSD0 supply voltage corrected to 1.8V. Sheet 19: JTAG signals changed to 3.3V through a buffer. Sheet 24: the “Other GPIOs” pins changed to 1.8V .
V1.0	25 April 2026	Sheet 5: R639 changed to an NTC, charging cutoff at 45 degrees C. R341 changed to 2.4K, charging current reduced to 430mA . Sheet 6: final power mode set to RTC ONLY + IO + DDR, with U6, U8, U10 and U39 removed. Sheet 7: U88 added and the USB hub power design reworked so that the 3.3V and 1.8V rails are powered only while Type-C is connected. Sheet 10: U60 removed, USB hub now reset directly from a GPIO. Sheet 18: U36 LoRa module removed, Wi-Fi power switch button added. Sheet 20: Power button added . D24 replaced with ESD0301L and a 220nF capacitor added for ESD protection. Sheet 24: J27 lost AB9/RGMII2_RD0/1V8 and gained a sensor 3.3V pin. Sheet 25: eMMC marked DNP . Minor passive adjustments across the schematic.
V1.0	28 July 2026	U36 to be mounted as required. PCB version number unchanged. This is the revision documented here.

Rev V1.0

The production release. Schematic BeagleBadge_V1.0_SCH_260728.pdf dated 28 July 2026, board file BeagleBadge_V1.0_260826.brd dated 26 August 2026, on a 6-layer 1.6mm PCB.

Three decisions in this revision change what a user can expect from the board and are worth reading before you buy or design against it:

- **eMMC is not populated.** The footprint is there. The device is not. See [eMMC footprint](#).
- **The GPIO expansion pads are 1.8V**, settled in V0.7. See [GPIO expansion header](#).
- **Charging is limited to 430mA** with a 45 degrees C NTC cutoff, which sets how quickly a BL-5C cell recharges. See [Battery charging and power path](#).

6.8 Mechanical Details

Board size, PCB stackup, mounting and the ePaper module outline are tabulated in [Dimensions and weight](#).

6.9 Pictures

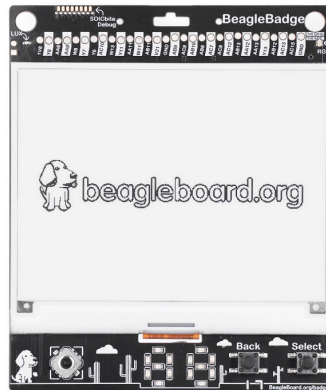


Fig. 6.1: BeagleBadge front

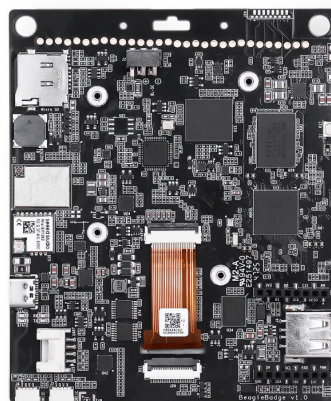


Fig. 6.2: BeagleBadge back

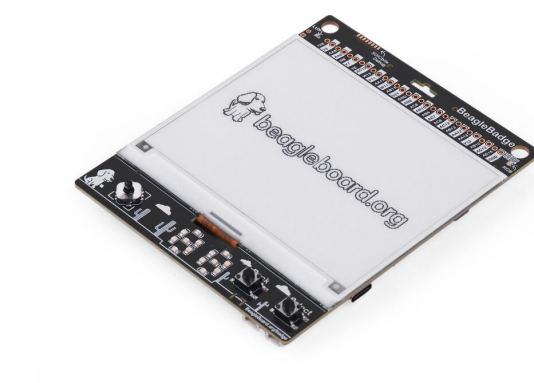


Fig. 6.3: BeagleBadge front at an angle

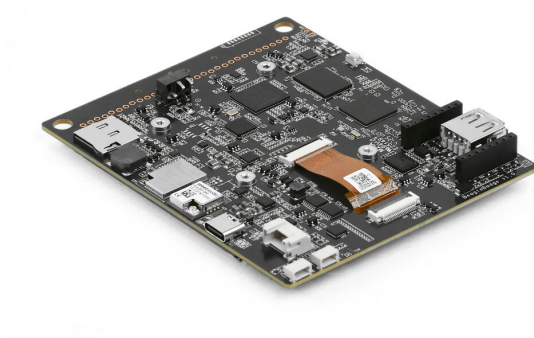


Fig. 6.4: BeagleBadge back at an angle